User's Guide

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For Safety information, Warranties, and Regulatory information, see the pages behind the index.

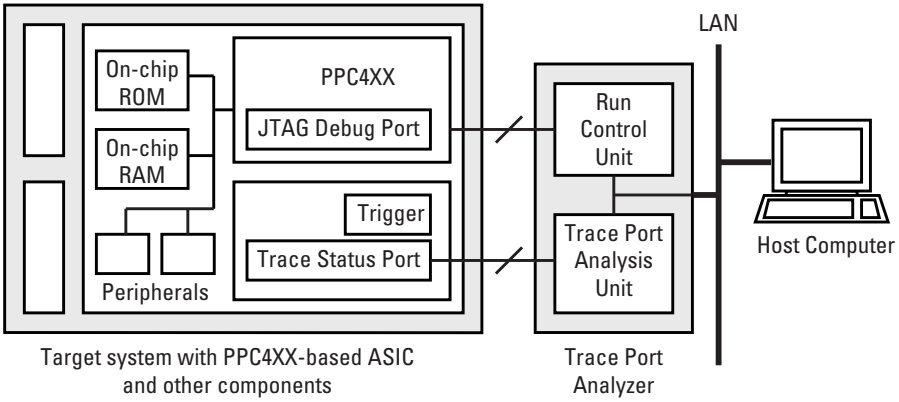
Agilent Technologies E5904B Option 060 Trace Port Analyzer for IBM PowerPC 4XX

Trace Port Analyzer —At a Glance

On-Chip Circuitry for Debugging

The PowerPC 400 family of microprocessors includes a trace port that outputs information about processor execution.

Software debuggers provide the user interface to the PowerPC 400 family processors; they configure the trace port using a run control unit (via the JTAG interface), and they display the data collected from the trace port.



Trace Port Analyzer Overview

The Agilent Technologies E5904B Option 060 Trace Port Analyzer contains:

- A run control unit.
- Circuitry for collecting output from the trace port, called the trace port analysis unit.
- A LAN interface for communicating with debuggers.

The Run Control Unit

In addition to configuring the trace port, the run control unit is also used for downloading code, starting/stopping processor execution, single-stepping through a program, setting breakpoints, and displaying/modifying registers and memory.

The Trace Port Analysis Unit

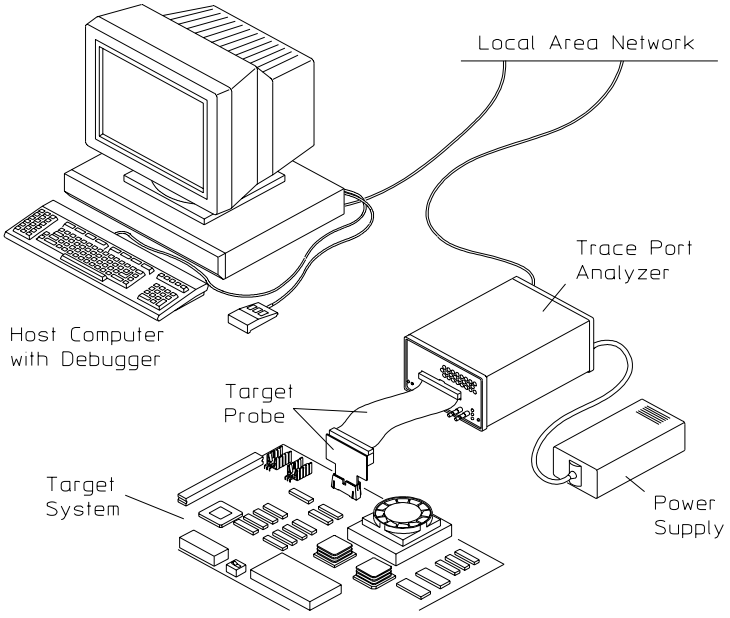
With the trace port analysis unit, you can:

- Capture trace data.
- Store up to 4M trace states.
- Capture data on trace ports whose voltages are between 1.8V and 5.0V.
- Send a trigger signal or a run control unit status signal to other instruments, or use signals received from other test instruments to stop processor execution or trigger the trace port analyzer.

The LAN Interface

With the IEEE 802.3 Type 10/100Base-TX LAN connection, you can:

- Connect the trace port analyzer to a target system in the lab and use debuggers anywhere else on the LAN.
- Connect to either 10 Mbps (10BASE-T) or 100 Mbps (100BASE-TX) twisted-pair ethernet LANs. (The trace port analyzer automatically negotiates the data rate for the LAN it is connected to.)



Debugger Software

A debugger must be used with the trace port analyzer. Debuggers such as RISCWatch from IBM, SingleStep from WindRiver, and others can be used.

The debugger user interface will let you:

- Download code, start/stop processor execution, single-step through a program, set breakpoints, and display/modify registers and memory.
- Set triggers, trigger sequences, etc. using the run control unit of the trace port analyzer.
- Collect trace information.
- Display execution flow and captured trace data.

Processors and ASIC Cores Supported

The Agilent Technologies E5904 Option 060 Trace Port Analyzer supports the following processors and ASIC cores with JTAG run control. Trace support is as listed below.

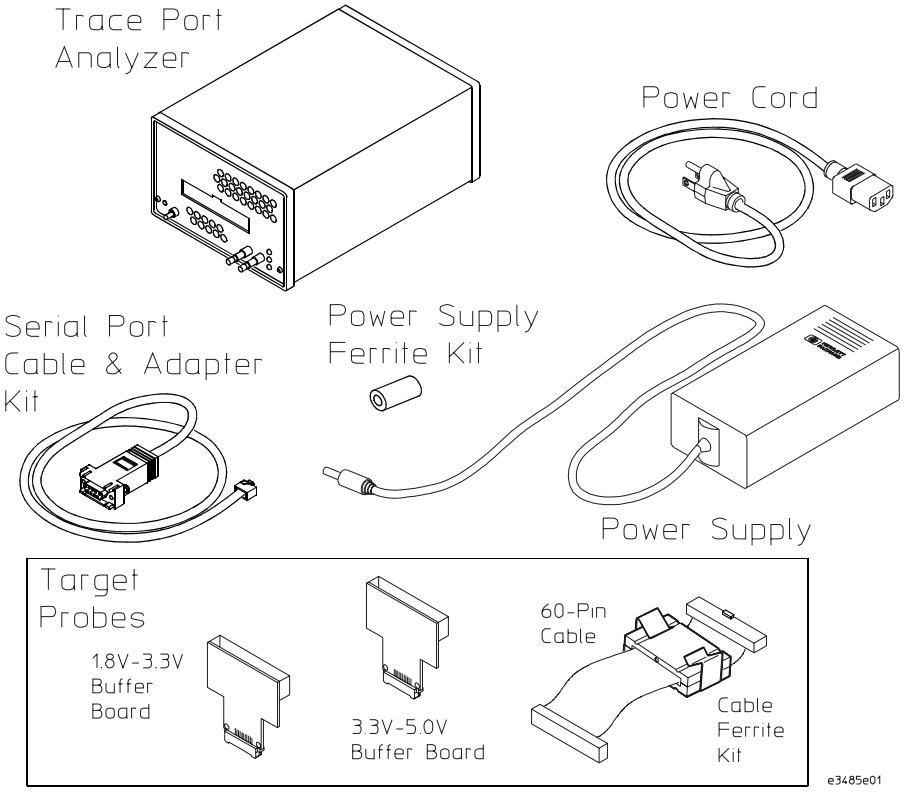
Processor	Trace Status Port
NPe405	Clock plus 8 trace status lines
440GP	Clock plus 15 trace status lines
405CR	Clock plus 8 trace status lines[1]
405GP	Clock plus 8 trace status lines[1]
403GCX	Clock plus 7 trace status lines
401GF	JTAG debug port only
403GA	Clock plus 7 trace status lines
403GB	JTAG debug port only
403GC	Clock plus 7 trace status lines

[1]GPIO pins 1-9 are used for both IO and trace.

Core	Trace Status Port
401x2	Clock plus 6 trace status lines
401A1	JTAG debug port only
405	Clock plus 8 trace status lines
440	Clock plus 15 trace status lines

Equipment Supplied

The Agilent Technologies E5904B Option 060 Trace Port Analyzer consists of:



Part number	Description
0950-3043	Power supply for trace port analyzer (marked F1044B)
E3483-68700	Ferrite kit for power supply
E5903-61601	60-pin cable
E3483-68700	Ferrite kit for 60-pin cable
E5903-66503	1.8 V - 3.3 V buffer board
E5903-66502	3.3 V - 5.0 V buffer board
E8130-68702	Serial cable and adapter
E3485-97000	This user's guide

In This Book

This is the User's Guide for the Agilent Technologies E5904B Option 060 Trace Port Analyzer. It describes:

- Target system design considerations and other requirements of the trace port analyzer.
- How to connect the trace port analyzer to a LAN, configure it, and connect it to the target system.
- How to coordinate measurements between the trace port analyzer and other test instruments.
- How to update trace port analyzer firmware.
- How to troubleshoot and solve problems.
- Characteristics of the trace port analyzer.

See Also

For information regarding the use of your debugger, see the user's guide manual supplied with your debugger.

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Target System Design Considerations

The quality and timing of the trace port signals to the trace port analyzer are critical for reliable operation. Some of the ASIC and printed-circuit board design issues to consider are:

- Output pad selection.
- Printed-circuit board trace lengths.
- Printed-circuit board trace termination.
- Setup and hold times for the trace data signals with respect to the trace clock.

The care that must be taken with the design of the trace port is generally proportional to the frequency of operation. At frequencies of more than 100 MHz careful SPICE analysis of the system, including the characteristics of the package should ideally be taken into account.

Early attention to the design guidelines can ensure correct operation of the trace port analyzer.

This chapter describes:

- Overview of signals
- A few ASIC design guidelines. More ASIC design guidelines may be available from the processor/core manufacturer.
- Printed-circuit board design guidelines.
- The header connector
- Height restrictions and keep-out requirements.
- Timing and voltage specifications for trace port signals.
- Header connector pinouts
- Buffer board voltage level requirements
- Buffer board modeling information

Trace Port Signal Overview

The trace port signals are described below.

TrcClk. Trace clock generated by the target processor.

TS[], ES[], BS[], and D0. These are trace status signals output from the processor or ASIC. See IBM's PowerPC 4XX user's guide for details.

VTRef. The VTRef signal is intended to supply a logic-level reference voltage to allow debug equipment to adapt to the signaling levels of the target board.

Outputs to target systems will be clamped at VTRef on high level outputs. Inputs from the target system will be sensed in reference to the VTRef voltage level.

NOTE: VTRef does NOT supply operating current to the debug equipment.

Target boards should supply a voltage that is between 1.8 V and 5.0 V. The target board should provide a sufficiently low DC output impedance that the output voltage not change by more than 1% when supplying a nominal signal current ±0.4 mA).

Debug equipment that connects to this signal should interpret it as a signal rather than a power supply pin and not load it more heavily than a signal pin. The recommended maximum source or sink current is ±0.4mA.

Signals for JTAG control

The following signals are required for JTAG (IEEE 1149.1 test access port) control.

nTRST. The nTRST signal is actively driven by the trace port analyzer to the Reset signal on the target JTAG port.

TDI. TDI is the Test Data In signal from the run control unit to the target JTAG port. It is recommended that this pin is pulled to a defined state.

TMS. TMS is the Test Mode Select signal from the run control unit to the target JTAG port. This pin must be pulled up on the target system to prevent the TAP (Test Access Port) state machine from exiting (TLR) test logic reset mode when the trace port analyzer is not connected to the target system.

TCK. TCK is the Test Clock signal from the run control unit to the target JTAG port. It is recommended that this pin is pulled to a defined state.

TDO. TDO is the Test Data Out from the target JTAG port to the run control unit.

Signals for Processor Control

$\overline{\text{SRESET}}$. This is an open collector output from the run control unit to the target system reset. This is also an input to the run control unit so that a reset initiated on the target may be reported to the debugger.

This pin should be pulled up on the target to avoid unintentional resets when there is no connection.

$\overline{\text{HALT}}$. This is an output from the run control unit to the target system. Active low.

ASIC Design Guidelines

ASIC Pad Selection and Placement

The position and type of pad selected is based on the following factors:

- Minimizing noise and coupling between trace and other signals.
- Ability to drive the external load.

It has been shown that the quality of the trace clock signal, as observed by the trace port analyzer, has the greatest effect on the reliability of the system. This is because it is vital that trace clock transition move cleanly through the threshold region of the input circuitry of the trace port analyzer, without glitches or ringing.

It has been observed that with certain types of package and pin placement the signal coupling between the trace data signals and the trace clock can be significant. If this is observed to be a problem during simulations, it is recommended that ground or static I/O signals are placed on both sides of the trace clock signal.

Contact the processor/core manufacturer for more ASIC design considerations.

Printed-Circuit Board Design Guidelines

Two cases need to be considered:

- A dedicated trace port. The trace port analyzer is the only load on the trace port signals.
- A shared trace port. The trace pins are shared with other functions; therefore, there are stubs on the printed-circuit board traces of the development board, and there is an increased load on the output driver.

Trace Port

Signal integrity at the trace port analyzer connector is very important. If you know the characteristics of your printed-circuit board traces, use the actual trace impedance and propagation delay.

If you do not have access to this information, a rough rule of thumb for microstrip (trace on outer layer over a ground plane) on FR4 printed-circuit board is a propagation speed of 63 ps/cm (160 ps/inch). The impedance of a 0.127 mm (0.005) inch wide trace as a microstrip is from 70 to 75 Ohms on a typical six-layer foil construction board. The impedance of a trace goes down as the width of the trace increases.

Knowledge of the characteristic impedance and signal edge rates of the target processor's or ASIC's trace port output drivers is necessary for proper design of the target system. Signals must be carefully routed from the target processor or ASIC to the trace port connector using high-speed design practices including using termination when necessary.

Also required is the actual setup and hold provided by the ASIC trace port outputs with reference to the trace clock. If you do not know the characteristics of the signals from your ASIC, consult your ASIC vendor. The variation between ASIC vendors on trace port output drivers and timing make it difficult to provide any general rule.

The output drive model for the Agilent trace port analyzer is provided in "Output Model" on page 125.

Printed-Circuit Board trace Length

Match all TS, ES, D0, BS, and TrcClk trace lengths between the processor or ASIC and the trace port connector within 100 ps. Overall differences of greater than 100 ps in trace lengths directly impact setup and hold requirements. If TrcClk is delayed compared to the data, the setup specification needs to be increased by the additional delay. If any data is delayed compared to the clock, the additional delay needs to be added to the setup requirement. If data paths are such that data has both greater than and less than delays compared with the clock, the difference needs to be added to both the setup and hold specification.

Signal Quality

Reflections, overshoot, and undershoot all need to be minimized to ensure accurate data acquisition. The primary variable is the rise time of a signal compared to its trace length. This is where the minimum signal rise and fall time becomes important.

The following points should be considered:

1. Ensure the one way propagation time for all traces is less than 1/3 of the signal rise time.

2. If traces must be longer than 1/3 of the signal rise time, then some form of signal termination is required. The recommended method is series termination. The series resistor must be placed as close as possible to the ASIC pin. The value of this series resistor, when added to the output impedance of the signal driver should closely match the impedance of the printed-circuit board trace. Certain processors include a series resistor in the trace output buffer—see the processor manufacturer's user's guide for details of processor output driver characteristics.

3. If series termination cannot be used, add parallel or matched AC termination on each signal trace at the trace port analyzer target header connector. This requires significantly more power from the ASIC, however, and the AC termination needs to closely match the frequency and rise time of the terminated signal. Therefore, in practice, parallel termination will rarely be possible.

4. If the total trace length is one rise time propagation delay or longer in length, follow standard high-speed design practices to minimize cross talk between the clock and the data signals.

Be aware that as the fabrication process for your ASIC improves, your output

driver will probably improve and your rise and fall times decrease. If you are close to violating the requirements of point 1, consider adding termination to the signals to ensure continued correct operation.

NOTE: Note that ASIC output pads which have an output impedance that is matched to the printed-circuit board trace may be available from your ASIC vendor. If these can be used, the signal quality of the trace port signals will be significantly improved.

Header Connector Requirements

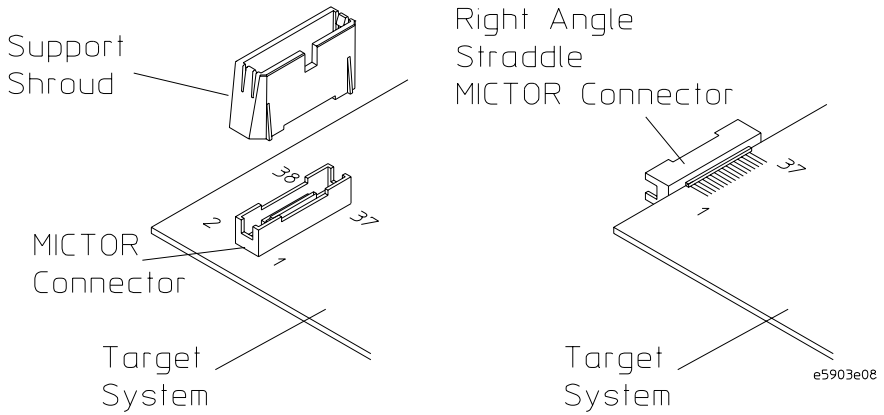
The target system header connector is an AMP MICTOR (*Matched Impedance ConnecTOR*) which has a 0.64mm (0.025") lead pitch. The header has 38 pins and is organized such that it can handle:

- 16 trace status port pins
- 1 trace clock pin
- 1 voltage reference pin
- 5 JTAG control pins
- 2 processor control pins

Recommended Orientation

The recommended trace port connector orientation is displayed in the following diagram.

Connector Orientation



There are two choices for the target header: a vertical connector, and a right angle straddle mount connector.

NOTE: The vertical connector is recommended because it can accommodate an optional support shroud that provides additional strain relief and thus greater reliability. The notch on the support shroud should be placed on the same side as the odd numbered pins on the MICTOR connector. The support shroud is

highly recommended.

The straddle mount connector should be used when board real estate is at a premium and there is no room for the vertical connector. A support shroud is not available for use with the straddle mount connector.

Connector and Support Shroud Part Numbers

The AMP part numbers for the MICTOR target headers are given below. These connectors may be purchased directly from AMP. Support shrouds and kits of five MICTOR connectors and support shrouds may be purchased from Agilent.

AMP MICTOR Headers Available from AMP

AMP Part Number	Description
2-767004-2	Vertical surface mount connector Ground bus lead length 1.397 mm (0.055″)
767054-1	Vertical surface mount connector Ground bus lead length 2.743 mm (0.108″)
767061-1	Vertical surface mount connector Ground bus lead length 3.505 mm (0.138″)
767044-1	Horizontal straddle mount connector

Support Shrouds Available from Agilent

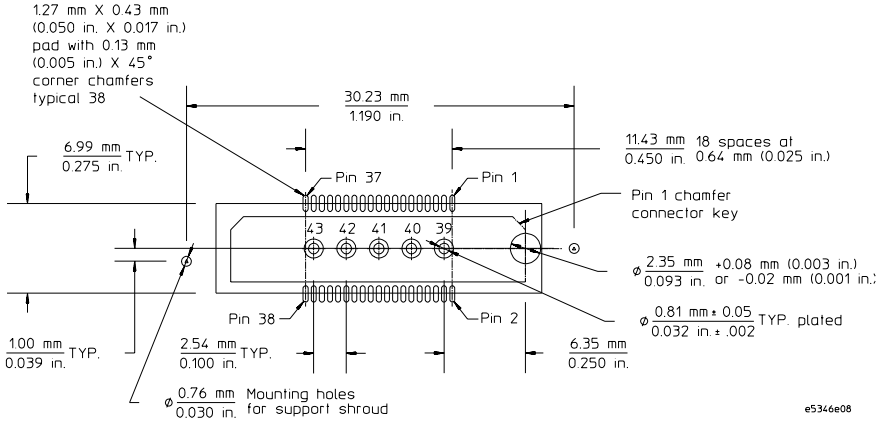
Agilent Part Number	Description
E5346-44701	Vertical support shroud for PCB thickness up to 1.575 mm (0.062″)
E5346-44704	Vertical support shroud for PCB thickness from 1.575 mm (0.062″) to 3.175 mm (0.125″)
E5346-44703	Vertical support shroud for PCB thickness from 3.175 mm (0.125″) to 17.780 mm (0.70″)

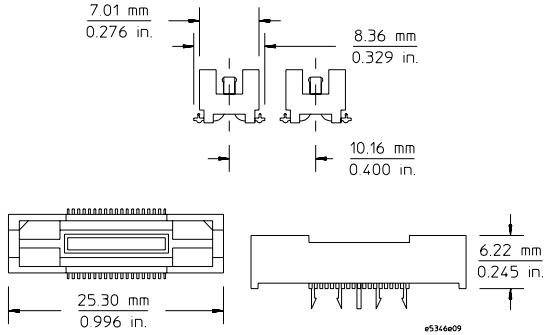
Set of Five MICTOR Connectors and Five Support Shrouds Available from Agilent

Agilent Part Number	Description
E5346-68701	Set of 5 MICTOR connectors and shrouds For PCB thickness up to 1.575 mm (0.062”)
E5346-68700	Set of 5 MICTOR connectors and shrouds For PCB thickness from 1.575 mm (0.062”) to 3.175 mm (0.125”)

Connector Dimensions

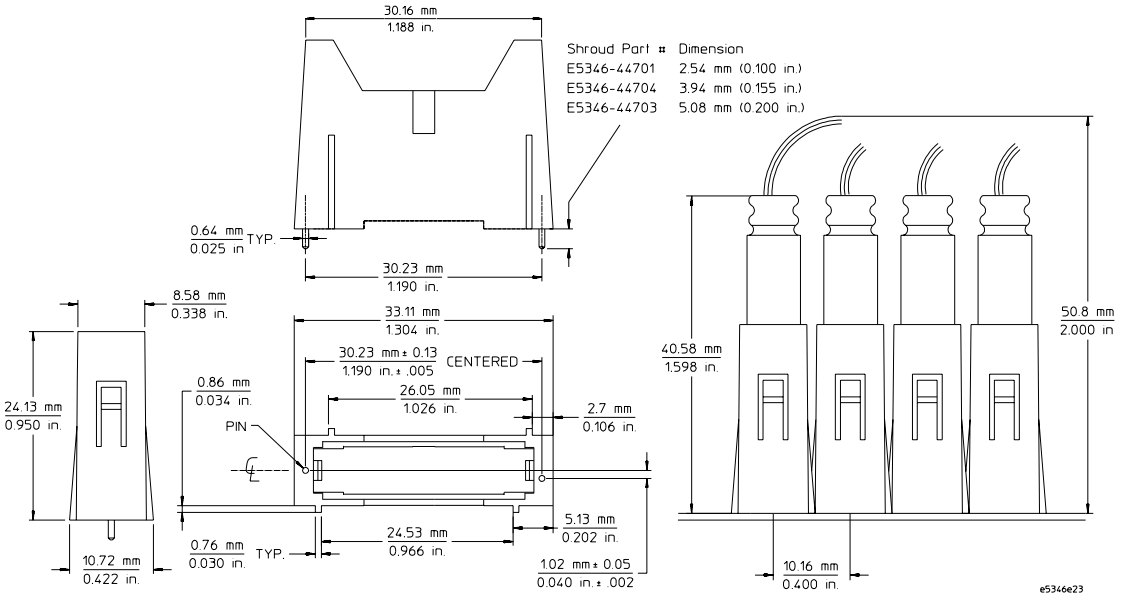
AMP MICTOR Connector Dimensions (AMP part # 2-767004-2)





Support Shroud Dimensions

Support Shroud Dimensions



Height Restrictions and Keep-Out Requirements

The Agilent Technologies E5904B Option 060 Trace Port Analyzer connects to the target MICTOR header with a small target probe (which consists of a 60-pin cable and a buffer board). The target probe connects either vertically or horizontally (to the edge of the target system PC board), depending on which MICTOR header you have installed on the target system.

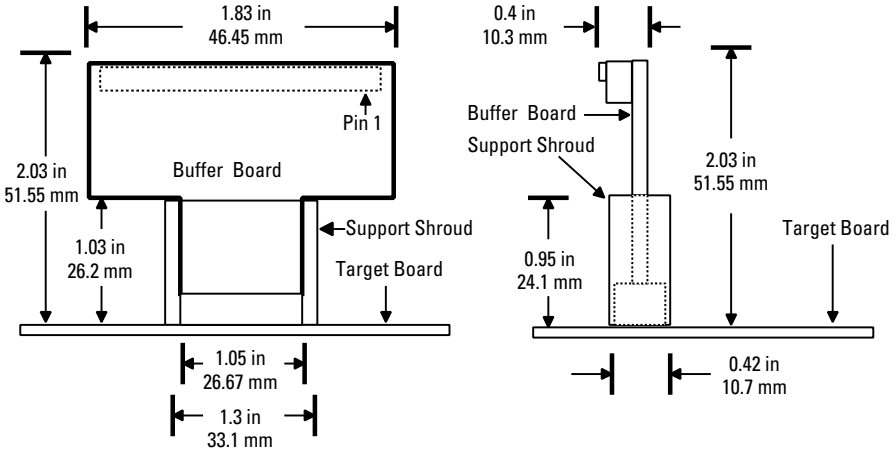
If the vertical header is used, make sure there is sufficient height clearance between the target system and any interface boards.

This section describes the height restrictions and keep-out for two target probes:

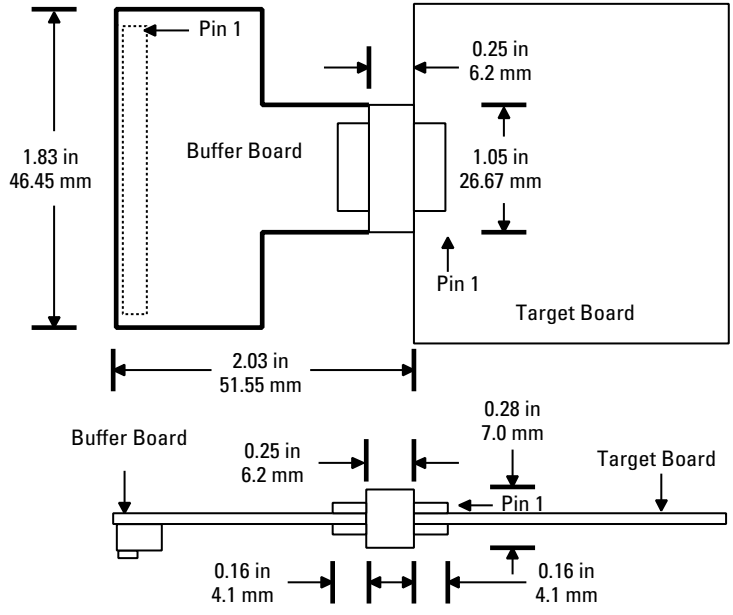
- The 1.8 V - 3.3 V buffer board (Agilent Part Number E5903-66503)
- The 3.3 V - 5.0 V buffer board (Agilent Part Number E5903-66502)

NOTE: The numbers silkscreened on the buffer boards will differ from the part number by one digit. For example: the E5903-66503 will be marked E5903-26503.

1.8 V - 3.3 V Buffer Board, Vertical Header, and Support Shroud Agilent Part Number E5903-66503

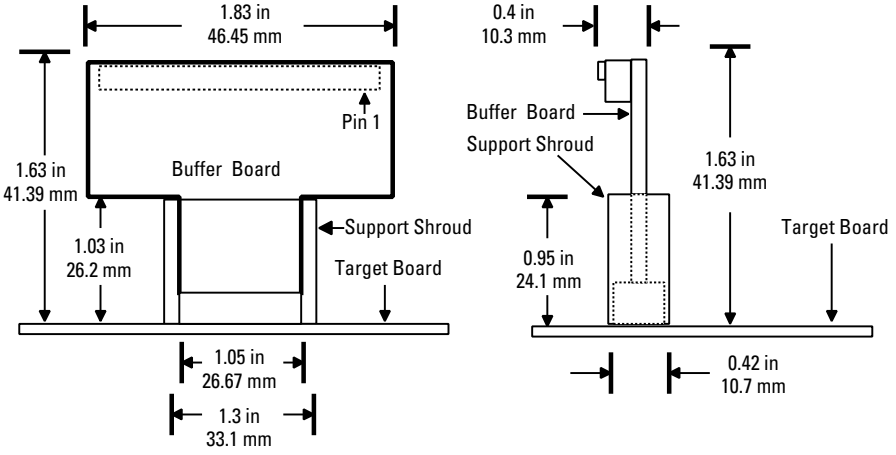


1.8 V - 3.3 V Buffer Board and Right Angle Connector Agilent Part Number E5903-66503

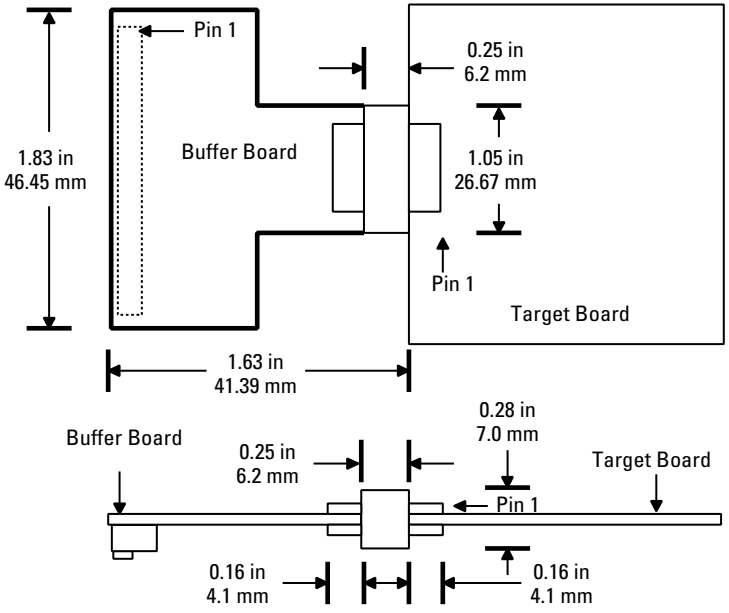


3.3 V - 5.0 V Buffer Board, Vertical Header, and Support Shroud

Agilent Part Number E5903-66502



3.3 V - 5.0 V Buffer Board and Right Angle Connector
Agilent Part Number E5903-66502



Target Header Connector Pin-Outs

The PowerPC 4XX family trace port defines the following target header pin-outs. If your target system has these pin-outs, use the included trace port analyzer buffer board.

PPC/MPC 401†/403/405 Target Header Connector Pin-Out

Target Header Pin-Out for the MICTOR Connector

	MICTOR Connector		
TS6 (DATA)	38	37	No Connect
TS5 (DATA)	36	35	No Connect
TS4 (DATA)	34	33	No Connect
TS3 (DATA)	32	31	No Connect
TS2e (STATUS - EVEN)	30	29	No Connect
TS1e (STATUS - EVEN)	28	27	No Connect
TS2o (STATUS - ODD)	26	25	No Connect
TS1o (STATUS - ODD)	24	23	No Connect
No Connect	22	21	nTRST
No Connect	20	19	TDI
No Connect	18	17	TMS
No Connect	16	15	TCK
No Connect	14	13	No Connect
Vref	12	11	TDO
No Connect	10	9	$\overline{\text{SRESET}}$
No Connect	8	7	$\overline{\text{HALT}}$
TrcClk	6	5	No Connect
No Connect*	4	3	No Connect*
No Connect*	2	1	No Connect*

† When using the 401GF or the 401A1 (without the trace status port) do not connect TS[1:6] pins.

* Pins 1, 2, 3, and 4 *must* be true no-connects; they are reserved for and may be driven by a logic analyzer.

PPC/MPC 440 Target Header Connector Pin-Out

Target Header Pin-Out for the MICTOR Connector

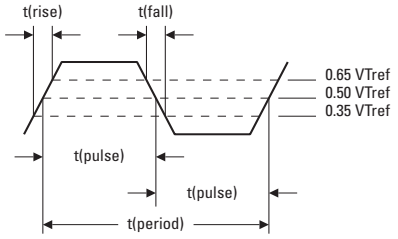
	MICTOR Connector		
TS6	38	37	ES3
TS5	36	35	ES2
TS4	34	33	ES1
TS3	32	31	ES0
TS2	30	29	BS2
TS1	28	27	BS1
TS0	26	25	BS0
ES4	24	23	D0
No Connect	22	21	nTRST
No Connect	20	19	TDI
No Connect	18	17	TMS
No Connect	16	15	TCK
No Connect	14	13	No Connect
Vref	12	11	TDO
No Connect	10	9	$\overline{\text{SRESET}}$
No Connect	8	7	$\overline{\text{HALT}}$
TrcClk	6	5	No Connect
No Connect*	4	3	No Connect*
No Connect*	2	1	No Connect*

NOTE: * Pins 1, 2, 3, and 4 *must* be true no-connects; they are reserved for and may be driven by a logic analyzer.

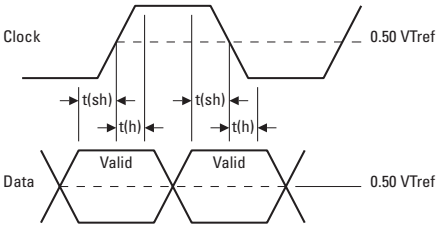
Timing and Voltage Specifications for Trace Port Signals

The signals from the target system to the trace port analyzer must meet certain timing and voltage requirements in order for the Agilent Technologies E5904B Option 060 Trace Port Analyzer to work correctly.

Signal Requirements



Clock Timing



Data Timing

Signal Requirements	
Maximum state clock frequency t(period) = 1/frequency	200 MHz (1.65 Volts to 3.6 Volts Target VTRef) 5 ns
Minimum clock pulse width, t(pulse)	2 ns (see note 1)
Maximum clock/data rise and fall time, t(rise) and t(fall)	3.6 ns (see note 1)
Minimum clock/data rise and fall time	See PCB guidelines
Data setup/hold times, t(su)/t(h)	1.5/1.0 ns (see notes 2 and 3)

NOTES:
1. Clock/data rise and fall times are measured between 35% and 65% of Target VTRef or +/- 30% of programmed threshold.
2. Setup/hold is measured at Target VTRef/2.
3. For “both edge” clocking, setup/hold must be met for both rising and falling edge of clock.

Required Voltage Levels: 1.8 V - 3.3 V Buffer Board

Absolute Maximum Ratings	Minimum	Maximum
Target VT_{Ref}	-0.5 V	4.6 V [1]
Clock and Data	-0.5 V	4.6 V [1]
Input Current (Input < -0.05 V)		-50 mA

[1] Minimum voltage can be exceeded if maximum current rating is observed.

Recommended Operating Range	Minimum	Maximum
Target VT_{Ref}	1.65 V	3.6 V
Clock and Data	0.0 V	3.6 V

DC Electrical Characteristics	Minimum	Maximum
Target VT_{Ref} range	1.65 V	3.6 V
V_{ih}	0.65 VT_{Ref}	
V_{il}		0.35 VT_{Ref}

Required Voltage Levels: 3.3 V - 5.5 V Buffer Board

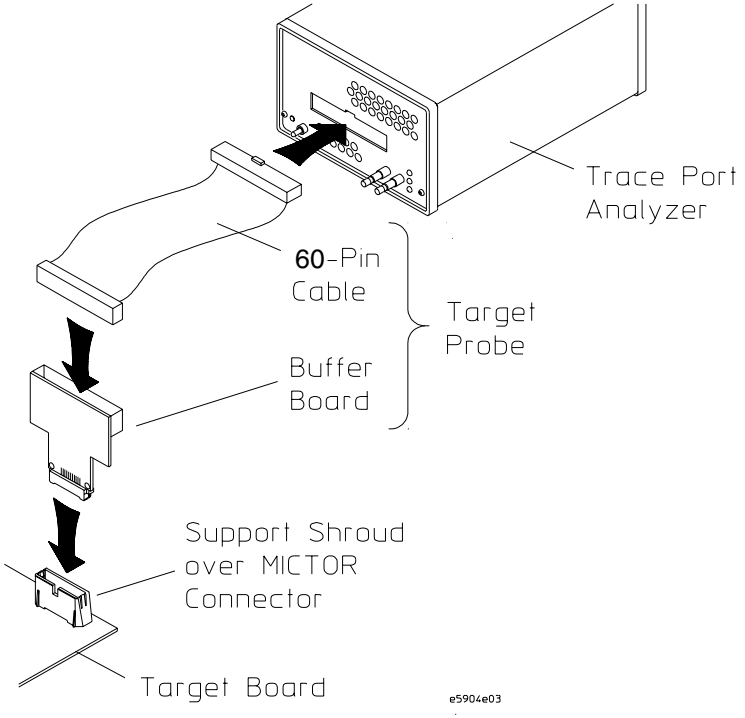
Absolute Maximum Ratings	Minimum	Maximum
Target VT_{Ref}	-0.5 V	5.5 V
Clock and Data	-0.5 V	7.0 V
Input Current (Input < -0.05 V)		-50 mA

Recommended Operating Range	Minimum	Maximum
Target VT_{Ref}	2.3 V	5.5 V
Clock and Data	0.0 V	5.5 V

DC Electrical Characteristics	Minimum	Maximum
Target VT_{Ref} range	2.3 V	5.5 V
V_{ih} (VT_{Ref} = 2.3 V to 2.7 V)	1.7 V	
V_{ih} (VT_{Ref} = 2.7 V to 5.5 V)	2.0 V	
V_{il} (VT_{Ref} = 2.3 V to 2.7 V)	-0.5 V	0.7 V
V_{il} (VT_{Ref} = 2.7 V to 5.5 V)	-0.5 V	0.8 V

Loading Effects

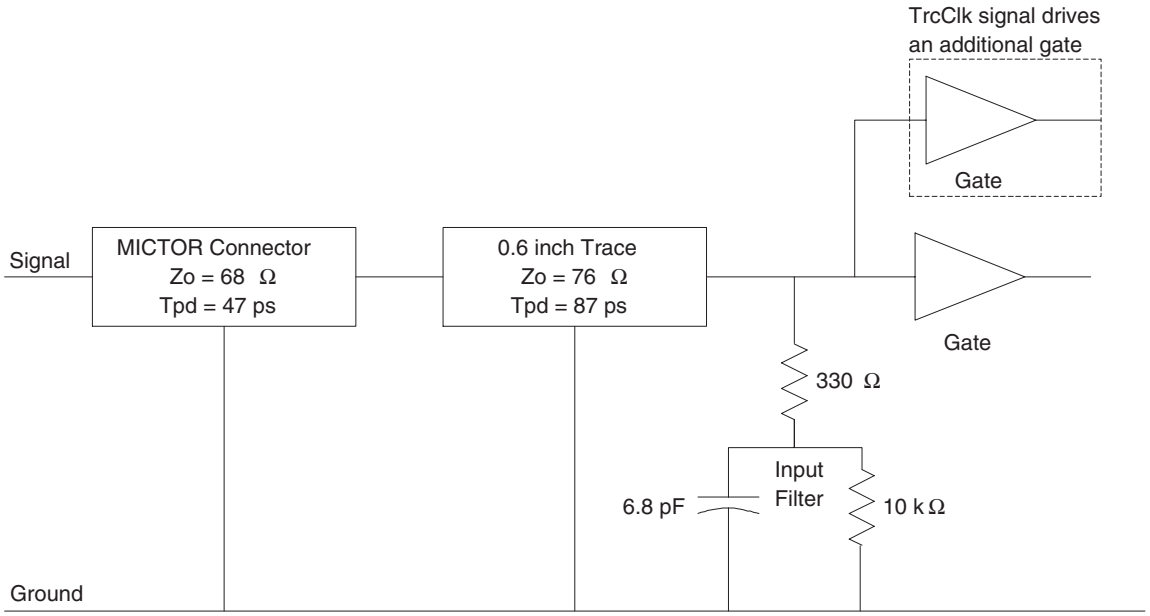
Target systems connect to the trace port analyzer via the target probe as shown below:



Target Probe Equivalent Load

The trace port analyzer presents the following equivalent load to each signal. Target systems must be capable of driving this load and meeting the signal requirements given on page 30.

Trace Port Analyzer Buffer Board—Equivalent Load Model



Buffer Board	Gate driven by target system
E5903-66503 (1.8 V to 3.3 V)	74AVC16834
E5903-66502 (3.3 V to 5.0 V)	74ALVT16827

Trace port analyzer probe characteristics (including target probe)	
Input resistance (DC)	10 kΩ ± 5%
Input capacitance, data inputs	4.0 pF
Input capacitance, clock input	6.5 pF

Modeling the Trace Port Analyzer Buffer Board

The following characteristics apply to both the 1.8 V - 3.3 V buffer board (Agilent Part Number E5903-66503) and the 3.3 V - 5.0 V buffer board (Agilent Part Number E5903-66502).

MICTOR Connector

- The MICTOR connector (right-angle plug to right-angle receptacle or right-angle plug to vertical receptacle) can be modeled as a transmission line with Z = 68 Ω and Tpd = 47 ps.

PC Board

- The trace port analyzer buffer board has the following characteristics:
  - trace width = 0.127 mm (0.005 inches)
  - trace thickness = 0.0178 mm (0.0007 inches)
  - microstrip trace for TS, ES, BS, D0, and TrcClk signals
  - distance from traces to ground plane = 0.178 mm (0.007 inches)
  - spacing between traces = 0.508 mm (0.020 inches)
  - ground plane thickness = 0.0356 mm (0.0014 inches)
  - trace length = 15.24 mm (0.6 inches)
  - Er = 4.8

or

- Zo = 76 Ω, Tpd = 87 ps

Input Filter

In place of the buffer board characteristics, you can use discrete models of 330 Ω, 6.8 pF, and 10 kΩ as shown below.

Undershoot/Overshoot

Undershoot and overshoot at the inputs to the buffer IC must be within the absolute maximum ratings shown in the tables on pages 31 and 32.

Buffer IC—1.8 V to 3.3 V Buffer Board

Use the IBIS model of a Philips 74AVC16834 IC in a TSSOP package. This model can be found on the Philips Semiconductor web site at:

http://www.philipslogic.com/support/ibis/avc/

The clock signal (TrcClk) is connected to two inputs of the buffer IC. Data signals are only connected to one input of the buffer IC.

Buffer IC—3.3 V to 5.0 V Buffer Board

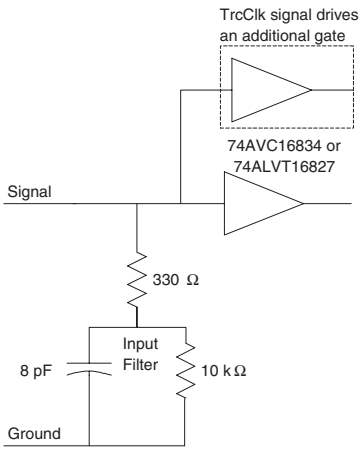
Use the IBIS model of a Philips 74ALVT16827 IC in a TSSOP package. This model can be found on the Philips Semiconductor web site at:

http://www.philipslogic.com/support/ibis/alvt/

The clock signal (TrcClk) is connected to two inputs of the buffer IC. Data signals are only connected to one input of the buffer IC.

Simplified Buffer Board Model

The following simplified discrete model of 330 Ω, 8 pF, 10 kΩ, and the gate (74AVC16834 for the 1.8 V - 3.3 V buffer board, or 74ALVT16827 for the 3.3 V - 5.0 V buffer board) can be used in place of the model previously presented.



2

Connecting to a Power Source

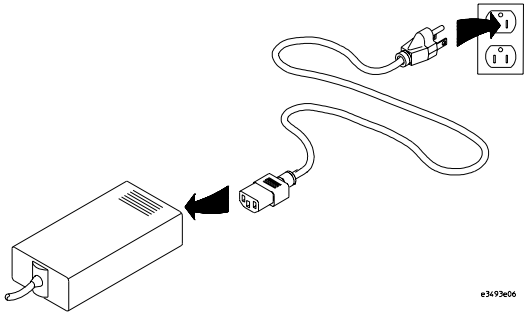
To connect the power supply

The trace port analyzer is shipped from the factory with a power supply and cord appropriate for your country. If the cord you received is not appropriate for your electrical power outlet type, contact your Agilent Technologies sales and service office (see “Contacting Agilent Technologies” on page 120).

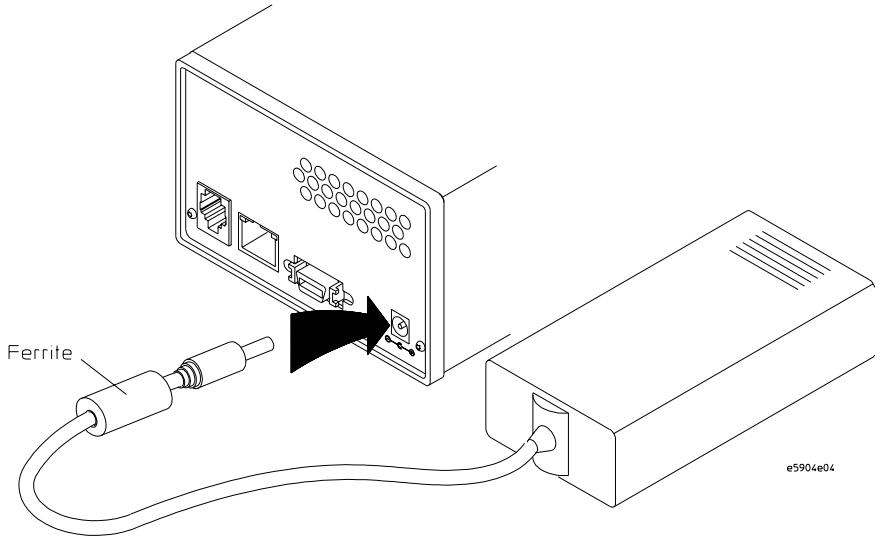
WARNING: Use only the supplied Agilent Technologies F1044B power supply and cord. Failure to use the proper power supply could result in electric shock.

CAUTION: Use only the supplied Agilent power supply and cord. Failure to use the proper power supply could result in equipment damage.

1. Install the ferrite on the 12V power cord, near the end which plugs into the trace port analyzer.
2. Connect the power cord to the power supply and to a socket outlet.



3 Connect the 12V power cord to the back of the trace port analyzer.

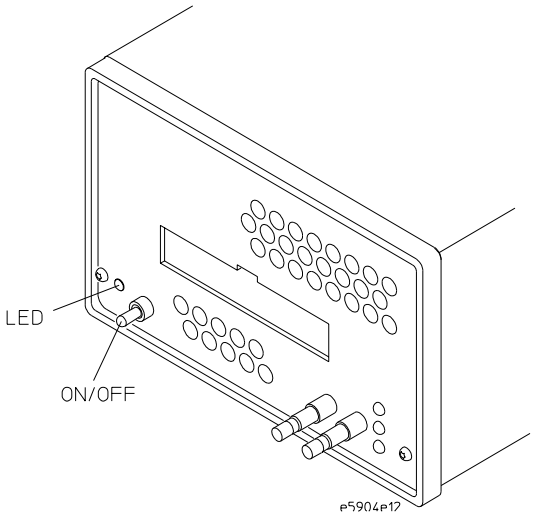


Ensure the power supply plug is completely seated in the power input receptacle.

To turn power ON

This procedure is for the trace port analyzer before it has been connected to a target system. (For the power ON procedure when connecting to a target system, see Chapter 6, “Connecting to a Target System,” on page 85.)

1 Turn ON the trace port analyzer power switch.



To turn power OFF

This procedure is for the trace port analyzer before it has been connected to a target system. (For the power OFF procedure when connected to a target system, see Chapter 6, “Connecting to a Target System,” on page 85.)

1 Turn OFF the trace port analyzer power switch.

3

Connecting to a LAN

The trace port analyzer must be connected to the LAN and set up with the proper LAN parameters so that a debugger can communicate with it.

The trace port analyzer has an IEEE 802.3 Type 10/100Base-TX LAN connector and is compatible with both 10 Mbps (10BASE-T) and 100 Mbps (100BASE-TX) twisted-pair ethernet LANs. (The trace port analyzer automatically negotiates the data rate for the LAN it is connected to.)

NOTE:

If the trace port analyzer is already active on the LAN and you wish to change its LAN parameters, you can use a "telnet" command on a networked computer to connect to the trace port analyzer; then, use the built-in "lan" command to change LAN parameters.

After making LAN parameter changes, you must cycle power to the trace port analyzer before the changes take effect. Doing this will break the network connection and end the telnet session.

Step 1. Decide on the LAN setup method

The trace port analyzer can be set up on the LAN (in other words, its LAN parameters can be configured) in two ways:

- By a DHCP (Dynamic Host Configuration Protocol) server that responds to BOOTP requests.
- By using a computer with terminal emulation software (or by using an actual terminal) connected to the trace port analyzer's serial (RS-232) port, and by entering commands to set the LAN parameters.

What is DHCP?

DHCP (Dynamic Host Configuration Protocol) allows clients (like the trace port analyzer) to obtain LAN parameters automatically from a server.

How does the trace port analyzer use DHCP?

The trace port analyzer uses "static allocation" (sometimes called "manual allocation") to obtain a permanent IP address. Every time the trace port analyzer is turned on, it sends out a BOOTP request packet. If the DHCP server on the network responds to BOOTP requests and has been configured to reply to the trace port analyzer's link-level address, it will respond with the IP address and other LAN parameters.

The trace port analyzer does not support "automatic allocation", which permanently allocates IP addresses from a pool of addresses.

Nor does the trace port analyzer support "dynamic allocation" of IP addresses—it does not track lease duration and request a new IP address when the lease is about to expire.

How does DHCP interact with other methods of setting LAN parameters?

Every time the trace port analyzer is turned ON, it sends out a BOOTP request packet (even if the LAN parameters have already been configured). As long as the DHCP server is configured to reply to BOOTP requests from the trace port analyzer's link-level address, it will respond with the IP address and other LAN parameters.

Step 2. Set the trace port analyzer's LAN parameters

- Find out whether port numbers 6470 and 6471 are already in use on your network and if that use constitutes a conflict.

  Computers on the network (running debugger software) communicate with the trace port analyzer through two TCP service ports. The default base port number is 6470. The second port has the next higher number (default 6471).

  In almost all cases, the default numbers (6470, 6471) can be used without change. If necessary, the base port number LAN parameter can be changed (using a serial port connection) if the port numbers conflict with some other product on your network.

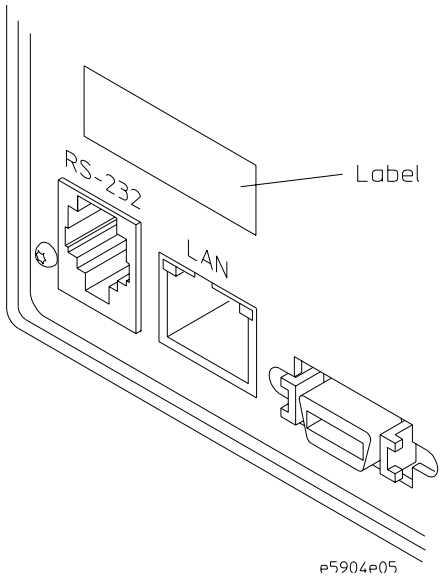
To set LAN parameters using DHCP

If there is a DHCP server on your network which responds to BOOTP requests and supports "static allocation" of IP addresses, it can be used to set the trace port analyzer's LAN parameters.

- Ask your system administrator to set up the IP address and other LAN parameters for the trace port analyzer on the DHCP server.

  You will need to supply the link-level address of the trace port analyzer.

  The link-level address (LLA) is printed on a label above the LAN connector on the trace port analyzer. This address is configured in each trace port analyzer shipped from the factory and cannot be changed.



To set LAN parameters using a serial port connection

The Agilent Technologies trace port analyzer has a 9600 baud RS-232 serial interface with an RJ12 connector.

The trace port analyzer is shipped with a serial cable (with RJ-12 connectors on both ends, with 6-wire straight-through connections) and an adapter (female RJ-12 to female 9-pin D subminiature). The adapter plugs into 9-pin serial ports found on most PCs.

Serial connections on a workstation

If you are using a UNIX® workstation as the host computer, you need to use a serial device file. If a serial device file does not already exist on your host, you need to create one. Once it exists, you need to ensure that it has the appropriate permissions so that you can access it. See the system documentation for your workstation for help with setting up a serial device.

Serial connections on a personal computer

Serial connections are supported on personal computers. (You must use

hardware handshaking if you will use the serial connection for anything other than setting LAN parameters.)

If you are using a personal computer as the host computer, you do not need to set up any special files.

1 Get the following information from your local network administrator or system administrator:

- An IP address for the trace port analyzer.

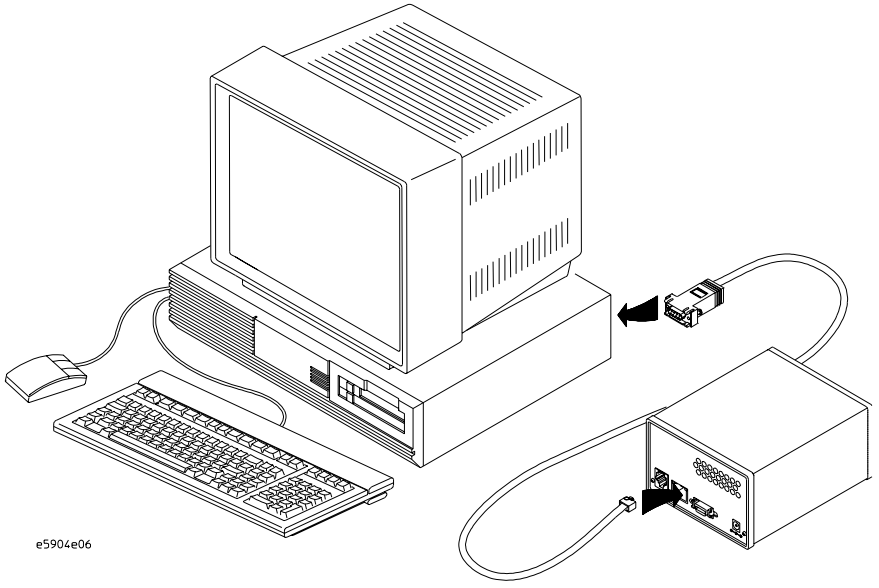
  You can also use a "LAN name" or "hostname" for the trace port analyzer, but you must configure it using the integer dot notation (such as 127.0.0.1).
- The gateway address.

  The gateway address is an IP address and is entered in integer dot notation. The default gateway address is 0.0.0.0, which allows connections only on the local network or subnet. If connections are to be made to workstations on other networks or subnets, this address must be set to the address of the gateway machine.
- The subnet mask.

  A subnet mask blocks out part of an IP address so that the networking software can determine whether the destination host is on a local or remote network. It is usually represented as decimal numbers separated by periods; for example, 255.255.248.0.

2 Connect the serial cable from the host computer to the trace port analyzer.

Use the DB9-to-RJ12 adapter and the serial cable supplied with the trace port analyzer.



3 Start a terminal emulator program on the host computer.

If you are using a personal computer, the HyperTerminal application in Microsoft Windows® will work fine.

If you are using a UNIX workstation, you can use a terminal emulator such as cu or kermit.

4 Configure the terminal emulator program for:

- Communication rate: 9600 baud
- Data bits: 8
- Parity: none
- Stop bits: 1
- Flow control: none

5 Turn on power to the trace port analyzer.

When the trace port analyzer powers up, it sends a version message to the serial port, followed by a prompt.

6 Press the Return or Enter key a few times.

You should see a prompt such as "p>" or "R>".

If you don't see a prompt, refer to "If there are serial port connection problems".

For information about the commands you can use, enter "?" or "help" at the prompt.

7 Display the current LAN parameter settings by entering the **`lan`** command:

```
R>lan
lan is enabled
   Link Status is UP
   100BaseTX
  lan -i 15.5.24.116
  lan -g 15.5.23.1
  lan -s 255.255.248.0
  lan -p 6470
  Ethernet Address : 08000909BAC1
R>
```

The Ethernet address, also known as the link level address, is preassigned at the factory, and is printed on a label on the trace port analyzer.

8 Change the LAN parameters by entering **`lan`** commands using the following syntax:

```
lan -i <internet> [-g <gateway>] [-p <port>] [-s
<subnet>]
```

The lan command parameters are:

`-i <internet>` The IP address which you obtained from your network administrator.

`-g <gateway>` The gateway address. Setting the gateway address allows access outside your local network or subnet.

`-s <subnet>` This changes the subnet mask.

`-p <port>` This changes the base TCP service port number, normally 6470.

Do not change the default port numbers (6470, 6471) unless they conflict with some other product on your network. The numbers must be greater than 1024. If you change the base port, enter the new value in the configuration of your debugger (and, for UNIX workstations, in the /etc/services file).

Example

To assign an IP address of 192.6.94.2 to the trace port analyzer, enter the following command:

```
R>lan -i 192.6.94.2
```

If there are serial port connection problems

If the trace port analyzer prompt does not appear in the terminal emulator window (or terminal display) after pressing the Return or Enter key:

❏ Make sure that you have connected the trace port analyzer to the proper power source and that the power switch is on.

With certain serial (RS-232) port interface cards, connecting to a serial port when the trace port analyzer is turned off (or is not connected) will hang the personal computer. The only way to get control back is to reboot the computer. Therefore, we recommend that you always turn on the trace port analyzer before attempting to connect via a serial port.

❏ Make sure the serial cable is connected to the correct serial port on your computer (or terminal).

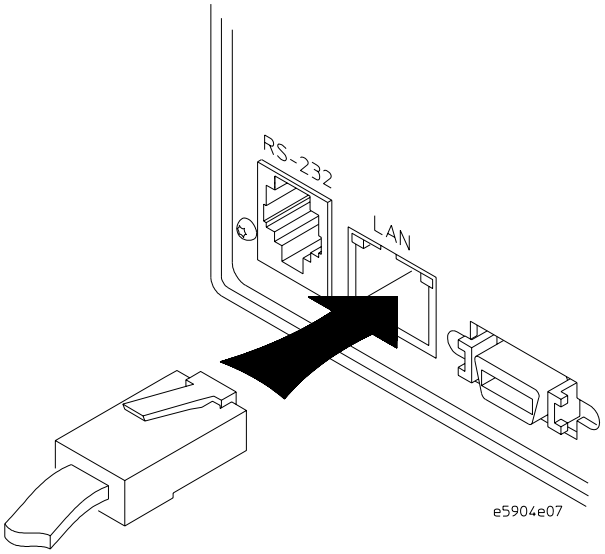
❏ Make sure you are using the serial cable and adapter which are supplied with the trace port analyzer.

❏ Make sure that you have properly configured the terminal emulator (or terminal) data communications settings:

- Communication rate: 9600 baud
- Data bits: 8
- Parity: none
- Stop bits: 1
- Flow control: none

Step 3. Connect the LAN cable

- Connect the LAN cable to the connector on the trace port analyzer.



Be sure to use the appropriate Category 3 or Category 5 cable for your LAN.

Step 4. Cycle power on the trace port analyzer

1. Cycle power on the trace port analyzer by powering it off then on again.

   When using DHCP, you must cycle power in order for the trace port analyzer to send out a DHCPDISCOVER packet so that its LAN parameter settings can be set automatically by a server.

   When using a serial connection, you must cycle power in order for the trace port analyzer's LAN parameter changes to take effect.

2. Wait at least 20 seconds for the trace port analyzer to recognize the LAN.

3. To verify that the trace port analyzer is now active and on the network, follow the instructions in the "Communicating with the Trace Port Analyzer" chapter.

4

Entering Commands

After the trace port analyzer has been connected to the LAN, there are two things you must do before you can configure the trace port analyzer:

- You must establish communications to the trace port analyzer from a networked computer.
- You must learn how to enter commands using the trace port analyzer's built-in command interface.

Establishing Communications over the LAN

Once the trace port analyzer has been connected to the LAN, it can communicate with computers on the network.

To use debugger software

The Agilent Technologies trace port analyzer can be used with several third-party debuggers.

Debuggers typically provide some way to enter commands in the trace port analyzer's built-in command interface.

- Refer to your debugger's documentation for information on accessing the trace port analyzer's built-in command interface.

If the debugger cannot communicate with the trace port analyzer

Some debuggers have an initialization file that needs to be properly defined before a debugger can connect to the trace port analyzer.

❏ Check that the debugger is using the correct IP address for the trace port analyzer.

Refer to your debugger manual for information on specifying the trace port analyzer's IP address.

❏ Telnet to the trace port analyzer from the same networked computer that runs the debugger software (see "To 'telnet' to the trace port analyzer").

If the telnet connection works, check that the debugger has the correct IP address for the trace port analyzer.

If the debugger uses the network *hostname* for the trace port analyzer (which doesn't work) and the telnet command uses the network *IP address* (which does work), the problem could be with the name server or host table lookup

mechanism. If this is the case, try using the trace port analyzer's IP address in the debugger.

If the telnet connection doesn't work, refer to "Verifying Trace Port Analyzer LAN Communications" in the "Solving Problems" chapter.

To "telnet" to the trace port analyzer

1 Verify your trace port analyzer is now active and on the network by issuing a telnet command from a networked computer to the trace port analyzer's IP address.

Example

```
$ telnet 192.35.12.6
R>
R>
```

If you do not see a prompt, press the Return or Enter key a few times.

This connection will give you access to the trace port analyzer's built-in command interface.

2 To enter a command, type it in at the built-in command interface prompt, and press the Return or Enter key.

For example, to view the LAN parameters, enter the "lan" command.

Example

```
R>lan
lan is enabled
   Link Status is UP
   10BaseT
  lan -i 130.29.66.134
  lan -g 130.29.64.1
  lan -s 255.255.248.0
  lan -p 6470
  Ethernet Address: 0030D300A10C
```

3 To exit from the telnet session, type Ctrl+D at the prompt.

If you cannot “telnet” to the trace port analyzer

❏ Refer to “Verifying Trace Port Analyzer LAN Communications” on page 106.

Using the Trace Port Analyzer's Built-In Commands

The trace port analyzer has a built-in command interface which you can use for configuring or troubleshooting the trace port analyzer.

You can access the built-in command interface via:

- A telnet (LAN) connection.
- A "debugger command" window in your debugger.
- A serial connection (as may have been used in "To set LAN parameters using a serial port connection" on page 45).

Command Prompts

The prompt indicates the status of the trace port analyzer:

U	Running user program
M	Running in debug mode
p	No target power
R	Trace port analyzer reset
r	Target reset
?	Unknown state
x	Run control disabled

Commonly Used Commands

Command	Description
b	Break—go into the background monitor state.
cf	Configuration—read or write configuration options.
help	Help—display online help for built-in commands
init	Initialize—**`init -c`** re-initializes everything in the trace port analyzer except for the LAN software. **`? init`** shows options.
lan	Configure LAN parameters.
m	Memory—read or write memory.
reg	Register—read or write a register.
mtest	Memory test—test target system memory.
r	Run—start running user code.
rep	Repeat—repeat a command or group of commands.
rst	Reset—reset the target processor.
s	Step—do a low-level single step.
ver	Version—display the product number and firmware version of the trace port analyzer.

Use **`? <command>`** (or **`help <command>`**) to show the command syntax and required parameters for each command. For example, enter **`? mtest`** to show syntax and required parameters for the memory test command.

Examples

To reset the trace port analyzer and break into the monitor, enter:

```
R>rst -m
```

To set register r0, and then view r0 to verify that it was set, enter:

```
M>reg r0=ffff
M>reg r0
  reg r0=0000ffff
```

To break execution and then step a single instruction, enter:

```
M>b
M>s
  PC=xxxxxxxx
M>
```

To determine what firmware version is installed in the trace port analyzer, enter:

```
M>ver
```

Online Help

Use **help *command_name*** to see the command syntax.

Example

To get help on the memory command, enter:

```
M>help m

  m - display or modify processor memory space

    m <addr>               - display memory at address
    m -d<size> <addr>      - display memory at address with display size
    m -a<size> <addr>      - display memory at address using access size
    m <addr>..<addr>       - display memory in specified address range
    m <addr>..             - display 128 byte block starting at address A
    m <addr>=<value>       - modify memory at address to <value>
    m -d<size> <addr>=<value>        - modify memory with display size
    m -a<size> <addr>=<value>        - modify memory using access size
    m <addr>=<value>,<value>         - modify memory to data sequence
    m <addr>..<addr>=<value>,<value> - fill range with repeating sequence

  NOTES: For display and access size descriptions see mo command
```

Note that some of commands listed in the help screens are generic commands and may not be available for your trace port analyzer.

5

Configuring the Trace Port Analyzer

After you have established communication between the trace port analyzer and networked computer (using a debugger or telnet software) and you've learned how to enter commands, you must set the trace port analyzer's configuration options appropriately for the target system.

You can save trace port analyzer configuration settings to a file so they can be used to re-configure the trace port analyzer at the beginning of each debugger session.

Using the Built-In "cf" Command

You can configure the trace port analyzer using the built-in "cf" commands.

1 Establish communications with the trace port analyzer over the LAN.

You can either telnet from a networked computer or you can use the debugger. For more information, refer to "Establishing Communications over the LAN" on page 55.

Debuggers typically provide some way to enter commands in the trace port analyzer's built-in command interface, or they provide a window for configuring the trace port analyzer.

2 Enter the built-in "**`cf`**" commands to view the current configuration settings.

Example

```
M>cf speed
  cf speed=12MHz
M>
```

3 Enter the "help cf" or "? cf" command to see a complete list of the configuration items that may be set.

Example

```
p>? cf

  cf - display or set emulation configuration

    cf                - display current settings for all config items
    cf <item>         - display current setting for specified <item>
    cf <item>=<value> - set new <value> for specified <item>
    cf <item> <item>=<value> <item> - set and display can be combined

  help cf <item>    - display long help for specified <item>

  --- VALID CONFIGURATION <item> NAMES ---
    rrt      - Restrict to real-time runs
    reset    - Configure reset actions
    speed    - Set JTAG clock
    frztmrs  - Select freeze timers option
    addrv    - Enable address validation
    mrdop    - Configure mem read operation
    dmwrop   - Configure D mem write operation
    imwrop   - Configure I mem write operation
    brfold   - Enable branch folding
    breakin  - Select SMB break input option
    trigout  - Select SMB trigger output option
    fastload - Enable fast memory loads
    vref     - Voltage reference
    thresh   - Voltage threshold
    trunas   - Trun autostop mode
```

4 To see a more detailed description of any configuration item, use the command "help cf <item>".

Example

```
M>help cf rrt

  Set restriction to real time runs

    cf rrt=no - (default)

       This option does not restrict to real time and will break into
       background temporarily if needed.

    cf rrt=yes

       This option restricts runs to real time which causes any command
       that requires a break to the monitor to be rejected except 'rst',
       'b', 'r' or 's'.
```

5 Use the **`cf`** commands to change the configuration settings (see "Setting the Configuration Options" on page 65).

See Also

For information on other built-in commands, see "Commonly Used Commands" on page 59.

Setting the Configuration Options

The configuration items must be set appropriately for each target system.

To specify whether runs are restricted to real-time

Value	Meaning	Built-in command
no	Allows commands which break to the monitor. Examples include commands which display memory or registers. These commands break to the monitor to access the target processor, then resume the user program.	cf rrt=no
yes	No commands are allowed which break to the monitor, except “break,” “reset,” “run,” or “step.” The processor must be explicitly stopped before these commands can be performed. (**Default**)	cf rrt=yes

If your debugger allows displaying or modifying memory or registers while the processor is running, you must set “rrt=no” in order to use this feature.

To specify the reset behavior

The reset configuration item controls what happens when a reset occurs.

Value	Meaning	Built-in command
core	A core reset resets the processor core, including the data and instruction caches. It does not alter the DMA controller, Bus Interface Unit or serial port (if one exists). The content of external DRAM is preserved since refreshes continue during reset. Device Control Registers (DCRs) are not affected by a core reset. A core reset stops the processor at address 0xFFFFFFFC.	cf reset=core
chip	A chip reset resets the entire chip including the core, caches, DMA Controller, Bus Interface Unit and serial port (if one exists). The content of external DRAM is not preserved since refreshes stop during and after the reset. A chip reset stops the processor at address 0xFFFFFFFC. (**Default**)	cf reset=chip
sys	A sys reset resets the entire chip with the same effect as a chip reset. In addition, the RESET signal is driven active (low) for a minimum of three clock cycles. A sys reset runs the processor from address 0xFFFFFFFC.	cf reset=sys
jtag	A jtag reset merely resets the JTAG port on the processor. It does not affect any of the processor resources or its state.	cf reset=jtag

Note that these actions occur only when the RESET signal is not asserted. Using the built-in **`rst`** command asserts RESET continuously until another command causes RESET to be negated.

To specify the JTAG clock speed

The trace port analyzer must be configured to communicate at a rate that is compatible with your target system processor. The JTAG clock speed (on the TCK signal) is independent of processor clock speed.

Value	Built-in command
11K - 50M	cf speed=*value*

The speed value can be a number followed by either K, which indicates the value is in kHz; or M, which indicates the value is in MHz. The clock can be set to speeds in the range 11 kHz to 50 MHz. Not all values in this range are valid; if an invalid speed is entered, the next slower valid speed will be used.

Showing the current speed setting

Entering **`cf speed`** without a value will display the current JTAG clock speed. The default speed for the PowerPC 4XX trace port analyzer is 32 MHz.

Configuring the Debug Port for Maximum Performance

The performance of the trace port analyzer depends on the speed at which it communicates with the target system. Better performance is obtained with faster communication speeds.

When to decrease TCK speed. Trace port analyzers are configured at the factory with a default TCK speed. In most cases, this is equal to the maximum allowable speed as specified by the manufacturer.

The default speed is suitable for most applications. However, the default speed is only valid if:

1. The processor is running at its full rated speed.
2. Trace lengths from the processor to the JTAG connector are short (two inches or less).
3. There are no stubs on the JTAG signals.

In some cases you may need to lower the TCK speed in order for the trace port analyzer to communicate reliably with the target system:

- When the target systems has additional loads on the JTAG lines.
- When the target system does not quite meet the requirements (as described in Chapter 1, “Target System Design Considerations,” on page 13).
- When you issue a break command and get the message "Unable to break".

When to increase TCK speed. Some target systems will allow TCK speeds greater than the default. The real maximum speed for a given target system can be determined empirically by increasing the speed and observing whether the communication to the target is reliable.

NOTE: Speeds greater than the default are not officially supported by Agilent Technologies or the chip manufacturer.

To set the freeze timers option

The freeze timers option determines how break, run, and step commands affect the state of timers.

Value	Meaning	Built-in command
yes	A break (stop) command will stop the processor and also freeze its timers. A run command will run the processor and will not change the state of the timers. A step command will step the processor and will not change the state of its timers.	cf frztmrs=yes
no (**Default**)	A break (stop) command will stop the processor and will not change the state of the timers. A run command will run the processor and unfreeze its timers. A step command will step the processor and will not change the state of its timers.	cf frztmrs=no

To enable or disable address validation

The address validation option can be used to check the validity of addresses prior to accessing memory.

Value	Meaning	Built-in command
yes	If yes, the driver checks the validity of addresses before it performs memory accesses. Valid memory addresses are either memory mapped on the chip's internal bus or defined by a bank register. A memory access to an invalid address will return an error message. (**Default**)	cf addrv=yes
no	If no, the driver does not check the validity of addresses. A memory access to an invalid address, in this case, will not return an error message but will cause a bus error on the processor.	cf addrv=no

Note that the yes setting is not valid for the 401GF or for 401 core-based processors.

To configure the memory read operation

Although PowerPC processors have one contiguous physical address space that can hold both data and instructions, it is necessary to differentiate between data spaces and instruction spaces when dealing with a memory/ cache coherency model during a write memory operation.

For mrdop=mm (memory model), a memory read from a cacheable address will return the contents of the data cache for the specified address. A memory read from a non-cacheable address will return the contents of physical memory.

For mrdop=phys, a memory read will always return the contents of physical memory. If the specified address is cacheable, the data cache will be turned off before the access and then turned back on after the access.

The memory read operation configuration entry defines how the memory and cache interact during a memory read operation. If both instruction and data caches are turned off, this configuration setting has no effect and a memory read will always return the contents of physical memory.

Memory read configuration

Value	Meaning	Built-in command
mm	A memory read from an address that is valid in either the data or instruction cache will return the contents of the cache. Memory reads from addresses not valid in either cache will return the contents of the physical memory.(**Default**)	cf mrdop=mm
phys	A memory read will always return the contents of physical memory.	cf mrdop=phys

Using the mrdop=phys setting with the cache enabled may show data that is no longer valid. Use this setting only for solving cache problems where you really need to see the contents of physical memory. For general operation, the "mm" setting should always be used.

To configure data memory write operations

Although PowerPC processors have one contiguous physical address space that can hold both data and instructions, it is necessary to differentiate between data spaces and instruction spaces when dealing with a memory/ cache coherency model during a write memory operation.

Only the memory write command allows specifying instruction or data memory operations. This may not be provided by your debugger interface. If not specified, memory write operations are always instruction memory.

If the data cache is disabled, a data memory write will always write to physical memory and this configuration setting is ignored.

Memory write configuration

Value	Meaning	Built-in command
mm (memory model)	Data writes to addresses that are valid in the data cache will write the value only to the cache and mark the cache line modified as "dirty", which will indicate to the CPU that the cache line must be written to memory. A data write that is not valid in the data cache will only be written to physical memory. (**Default**)	cf dmwrop=mm
thru	A data memory write to an address that is valid in the data cache will write to both cache and physical memory. If the address is not valid in the cache, only physical memory will be modified.	cf dmwrop=thru
bypass	A data memory write to a cacheable address will first turn off the data cache, write the value to physical memory, then turn on the data cache. A data memory write to a non-cacheable address will write to physical memory.	cf dmwrop=bypass

The **cf dmwrop=bypass** setting should be used with extreme caution because dirty cache entries may be written by the processor over the new data value written to memory by the trace port analyzer.

To configure instruction memory write operations

Although the PowerPC processor has one contiguous physical memory address space that can hold both data and instructions, it has separate caches for instructions and data. These separate caches must be considered in order to keep the caches and memory coherent during memory write operations. Code download always writes to physical memory and disables any cache entries containing addresses written for improved performance. Some host interfaces use the code download mode for all memory write operations so this setting may or may not have any effect on your debugger.

Only the memory write command allows specifying instruction or data memory operations. Access to this may not be provided by your debugger interface. If not specified, memory write operations are always instruction memory.

If the instruction and data caches are both disabled, an instruction memory write will always write to physical memory and this configuration setting is ignored. If the instruction cache is disabled, instruction memory writes will always write to physical memory and the data cache will be either updated or bypassed, depending on this configuration setting.

This configuration setting controls the behavior of both caches when doing instruction memory writes so that instruction memory writes can be used for all memory operations, if desired.

Instruction memory write configuration

Value	Meaning	Built-in command
upd_dcb	This stands for instruction cache update, data cache bypass. An instruction memory write to an address that is valid in the instruction cache will write the value to both the instruction cache and memory. The data cache will be bypassed even if the address is valid in the data cache.	cf imwrop=upd_dcb
upd_dcu	This stands for update instruction cache and data cache update. An instruction memory write to an address that is valid in both caches will write the value to both caches and physical memory. (**Default**)	cf imwrop=upd_dcu
inv_dcb	This stands for instruction cache invalidate and data cache bypass. An instruction memory write will invalidate the instruction cache if valid and write only to physical memory. The data cache is not modified even if valid.	imwrop=inv_dcb
inv_dcu	This stands for instruction cache invalidate and data cache update. An instruction memory write will invalidate the instruction cache if valid and write to physical memory. The data cache will also be updated if the address is valid in the data cache	imwrop=inv_dcu

To enable branch folding

This configuration item controls trace port analyzer behavior when stepping through assembly language branch instructions.

Branch Folding Configuration

Value	Meaning	Built-in command
yes	The processor is allowed to fold branches and cr logicals during stepping and running. Folding a branch results in an automatic jump to the branch location upon encountering a branch instruction. (**Default**) Note: This setting is not valid for the 401GF or for 401 core-based processors.	cf brfold=yes
no	The processor is not allowed to fold branches and cr logicals during stepping and running. When a branch instruction is encountered, program execution will stop at the branch instruction rather than automatically evaluating the branch instruction and jumping to the location specified.	cf brfold=no

To configure the Break In SMB port

The Break In SMB connector is located on the front of the trace port analyzer. The cf breakin configuration item controls how the trace port analyzer responds to an input at the Break In SMB port.

Value	The Break In SMB will	Built-in command
off	Inputs to the Break In SMB will be ignored.	cf breakin=off
rising	SMB breaks are enabled. A rising edge at the SMB input will stop the processor (break to monitor mode). If the edge is applied while the trace port analyzer is scanning the processor, the trace port analyzer will respond after it has completed scanning the processor. (**Default**)	cf breakin=rising
falling	A falling edge at the SMB input will cause the trace port analyzer to stop the processor (break to monitor mode). If the edge is applied while the trace port analyzer is scanning the processor, the trace port analyzer will respond after it has completed scanning the processor.	cf breakin=falling

NOTE: Inputs at the break in SMB are acted upon only when the processor is running. Inputs at the break in SMB will be ignored if the processor is reset or in monitor (debug mode).

See Also See Chapter 7, “Coordinating Measurements with Other Test Instruments,” beginning on page 91 for more information.

To configure the Trigger Out SMB port

The Trigger Out SMB connector is located on the front of the trace port analyzer. The cf trigout configuration item controls how the trace port analyzer drives the SMB Trigger Out port.

Value	The Trigger Out SMB will	Built-in command
fixhigh	Always be high	cf trigout=fixhigh
fixlow	Always be low	cf trigout=fixlow
monhigh	Go high when the processor is stopped. (**Default**)	cf trigout=monhigh
monlow	Go low when the processor is stopped.	cf trigout=monlow

To enable fast memory loads

Fast Memory Loads Configuration

Value	Meaning	Built-in command
yes	Enable fast target memory load. (**Default**)	cf fastload=yes
no	Use normal memory load routine.	cf fastload=no

When the trace port analyzer is configured for fast memory loads it ignores memory write coherency options (cf imwrop and cf dmwrop) in order to improve performance while loading memory. Instead of following the coherency model specified by the imwrop or dmwrop configuration entries, the trace port analyzer turns off both caches, invalidates the instruction cache and flushes the dcache, then begins the load. Once the load is complete, the cache configuration registers are returned to their original states.

The fast memory write configuration gains much of its speed by ignoring unusual cases that the slower memory write function must handle. Specifically, fast memory load can not be used if data is not word aligned, data access size is not set to 4, or if the MMU or debug wait mode are enabled. If any of these conditions are true, slow memory write will be used regardless of the setting of this configuration item.

The **`cf fastload=no`** command can be issued if the user wants the load command to follow memory write coherency options or if there are problems with the fast memory write routines on particular targets.

To configure the voltage reference

The trace port analyzer normally uses the VTRef signal on the JTAG connector to determine logic high and logic low levels when driving the TDI and TCK signals.

However, you can specify that the trace port analyzer use an internally generated voltage reference instead, when:

- The target system connector does not have the correct voltage on the VTRef pin, or
- You have some other non-standard situation.

Value	Meaning	Built-in command
external	The voltage reference is generated by the target system and is found on the VTref pin of the header connector. (**Default**)	cf vref=external
value	The voltage reference of *value* is generated internally by the trace port analyzer. The value is a number followed by either mV, which indicates the value is in millivolts, or V, which indicates the value is in volts.	cf vref=*value*

CAUTION: The cf vref=value option should only be used if the core voltage is different than that of the Vref signal on the JTAG connector. Use this option with extreme care, because it is possible to damage the target system if the voltage level is chosen incorrectly.

To configure the threshold voltage

The trace port analyzer normally uses 1/2 of VTref as its threshold voltage. You can specify that the trace port analyzer use a different threshold voltage.

Voltages above the threshold will be considered logic high and voltages below this level will be considered logic low.

Value	Built-in command
1/2	cf thresh=1/2 (**Default**)
2/3	cf thresh=2/3
1/3	cf thresh=1/3

If the voltage reference is set to "external," the threshold will be calculated with respect to the voltage on the VTref pin of the target header connector.

If the voltage reference is not set to "external," the threshold will be calculated with respect to the "**`value`**" chosen in the **`cf vref=value`** command. See "To configure the voltage reference" on page 80

To configure the autostop mode

Value	Meaning	Built-in command
yes	If yes, a trace measurement that results in a complete measurement will automatically stop the processor.	cf trunas=yes
no	If no, a trace measurement that results in a complete measurement will not stop the processor. (**Default**)	cf trunas=no

To save and restore configuration option settings

NOTE: The configuration option settings on the preceding pages can be stored using the `cfsave -s` command. The configuration option settings that use the "tcf" commands on the following pages will not be saved with the `cfsave -s` command.

- Use the "cfsave -s" command to store all configuration option settings in the trace port analyzer's flash memory.
- Use the "cfsave -r" command to restore the most recently saved configuration option settings.

  If the trace port analyzer is re-initialized, it will return to all the default configuration option settings. You can use the "cfsave -r" command to restore the configuration option setting that were last saved.

6

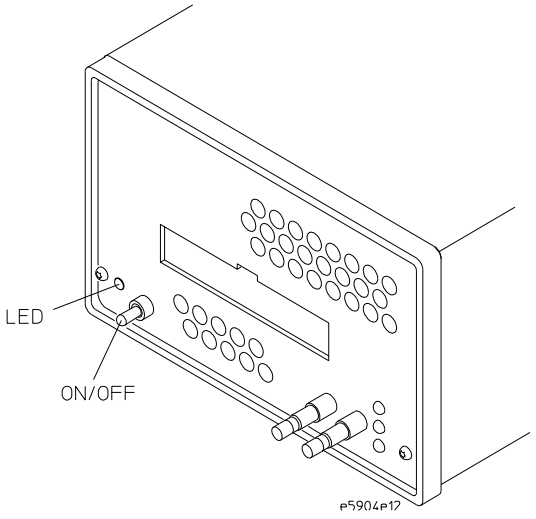
Connecting to a Target System

After the trace port analyzer has been properly configured for the target system, you can connect it to the target system and verify its operation.

Connecting the Trace Port Analyzer to the Target System

Step 1. Turn OFF power to the target system.

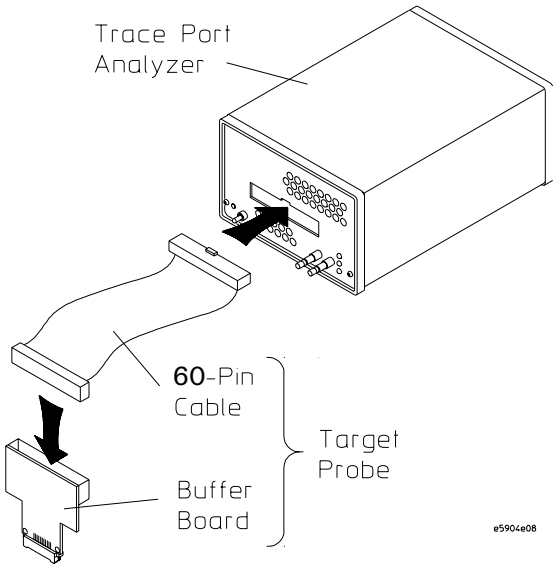
Step 2. Turn OFF the trace port analyzer power switch.



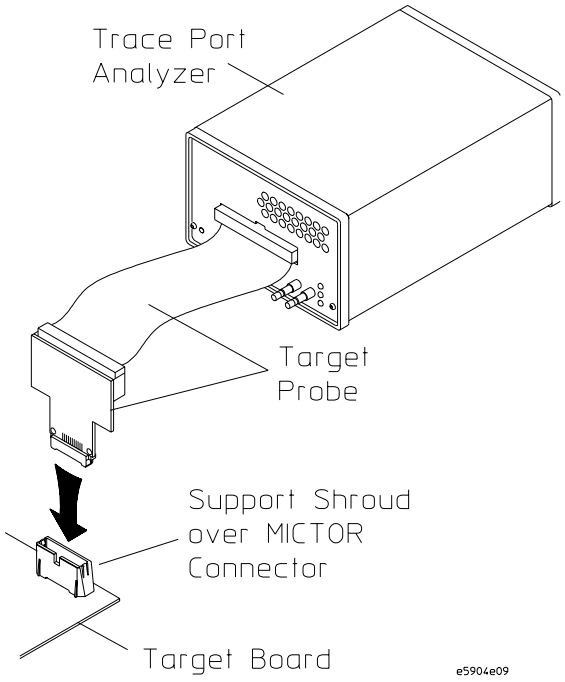
Step 3. Connect the trace port analyzer to the target probe.

Plug one end of the 60-pin cable into the trace port analyzer.

Plug the other end of the 60-pin cable into the connector on the buffer board.



Step 4. Plug the target probe into the target system MICTOR header connector.



Step 5. Turn ON the trace port analyzer power switch.

Step 6. Turn ON the target system power switch.

Verifying the Target System Connection

After the trace port analyzer has been plugged into the target system, you should verify that the trace port analyzer works correctly.

To verify trace port analyzer operation

❏ Perform some simple tests in the debugger to verify that the trace port analyzer is working properly with the target system.

If the trace port analyzer doesn't work with the debugger

Most problems are associated with not having the trace port analyzer and target system properly configured or initialized.

❏ Initialize the trace port analyzer and target system so that the debugger can connect.

Refer to your debugger manual for proper initialization.

If there are target system interaction problems

❏ See "Verifying Run Control Interaction with the Target System" on page 111.

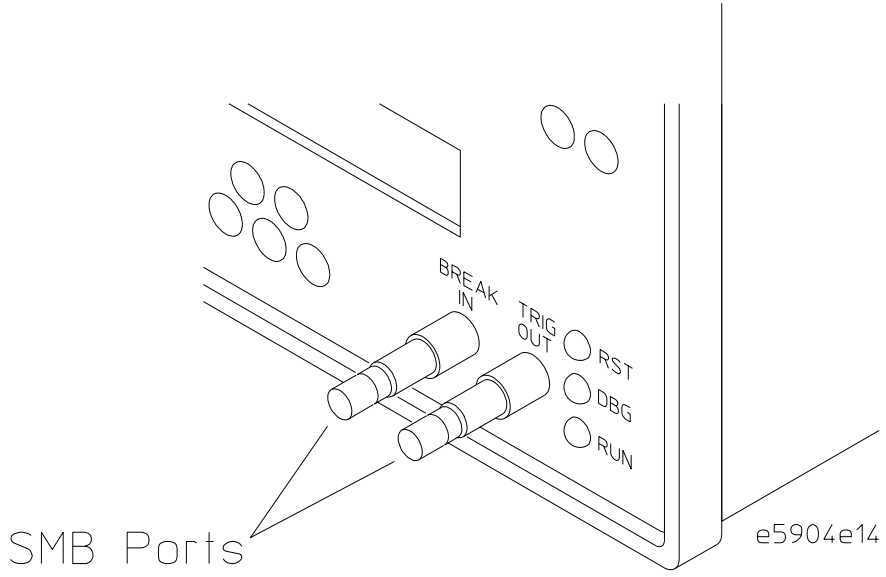
7

Coordinating Measurements with Other Test Instruments

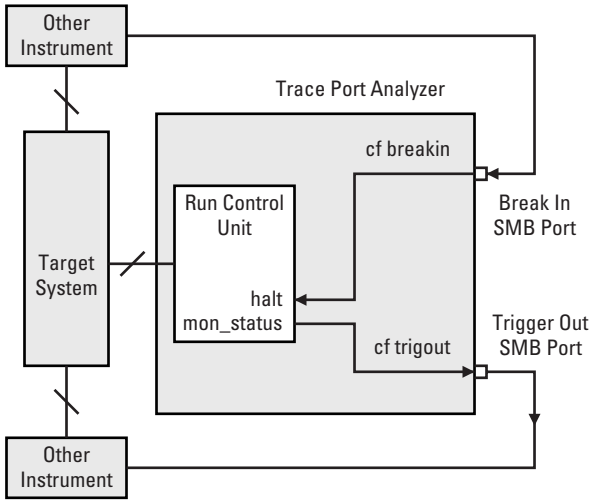
You can make coordinated measurements when you want to correlate real-time trace data from the processor's JTAG trace port with data captured by other test instruments (for example, a logic analyzer that captures data from other parts of your target system).

The Agilent Technologies E5904B Option 060 trace port analyzer has two SMB ports for coordinating measurements with other test instruments:

- Trigger Out SMB port.
- Break In SMB port.



By using the trace port analyzer's "trigout" and "breakin" configuration options, you can route the Trigger Out and Break In signals to the run control unit.



Receiving a Break In Signal from Another Test Instrument

You can use the trace port analyzer's Break In signal to allow another test instrument to halt processor execution (in other words, make the run control unit run in its monitor).

To halt processor execution

When another test instrument detects a problem, you might want to stop processor execution, for example, to examine registers and variable values or to begin stepping through processor execution.

1. Connect the other test instrument's output to the trace port analyzer's Break In SMB port.
2. Set the trace port analyzer's "breakin" configuration item to either "rising" or "falling" (depending on whether the other test instrument outputs a rising edge or a falling edge).
3. Start the processor's execution using the run control unit.
4. Start the other test instrument's measurement.

See Also "To configure the Break In SMB port" on page 77.

Driving a Trigger Out Signal to Another Test Instrument

You can use the trace port analyzer's Trigger Out signal to indicate to another test instrument when processor execution stops (in other words, when the run control unit is in its monitor).

To indicate when processor execution stops

You might want to do this, for example, to qualify a (synchronous) state logic analyzer's sampling clock so that it captures data only when the processor is executing the target program (and not when the debugger is using the run control unit to read and write memory locations).

1. Connect the trace port analyzer's Trigger Out SMB port to the other test instrument's input.
2. Set the trace port analyzer's "trigout" configuration item to either "monhigh" or "monlow" (depending on whether the other test instrument expects an active high or an active low signal).
3. Start the other test instrument's measurement.
4. Control the processor's execution with the run control unit.

See Also

"To configure the Trigger Out SMB port" on page 78.

8

Updating Firmware

If there is a newer version of firmware for the Agilent Technologies E5904B Option 060 trace port analyzer, you can update it using the procedures described in this chapter.

To display current firmware version information

1. Use the "telnet" command from a networked computer to access the trace port analyzer's built-in command interface.
2. Enter the built-in "ver" command to view the version information for firmware currently in the trace port analyzer.

Example

```
p>ver

         Copyright (c) Agilent Technologies, Inc. 1999
         Copyright (c) International Business Machines Corp. 1995
All Rights Reserved.  Reproduction, adaptation, or translation without prior
written permission is prohibited, except as allowed under copyright laws.

  HPE8130A Series Emulation System
    Version:   A.01.10 16May01
    Location:  Generics

  HPE3495A PowerPC 400 JTAG Emulator
    Version:   A.05.07 31May01
p>
```

To get firmware from the web

To update the firmware, you must have access to the World Wide Web and a personal computer or a workstation connected to your trace port analyzer.

1. Download the new firmware from the following World Wide Web site:

   http://www.cos.agilent.com/probe/

2. Follow the instructions on the web site for installing the firmware.

To update firmware from a floppy disk

- Follow the instructions on the README file on the floppy disk.

  The firmware can be installed using either a personal computer or a workstation which can read personal computer floppy disks.

9

Solving Problems

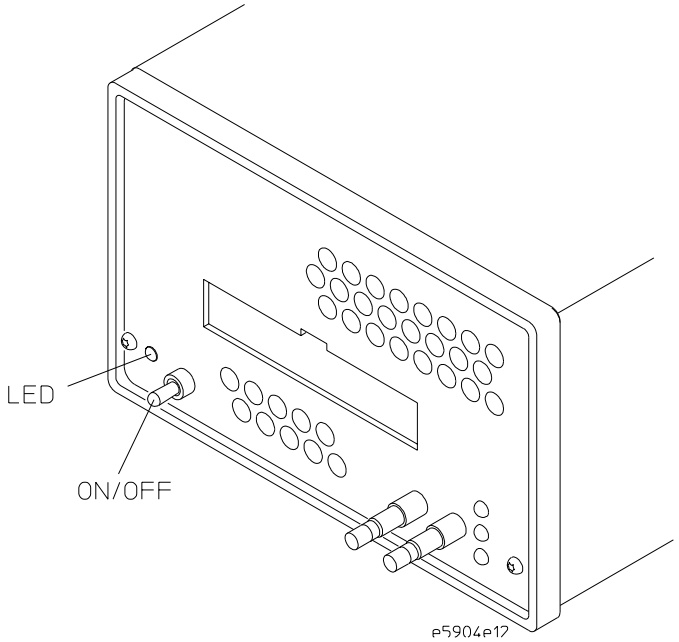
Problems with the trace port analyzer can occur in:

- The connection between the trace port analyzer and the debugger.
- The trace port analyzer itself.
- The connection between the trace port analyzer and the target system.
- The target system.

You can use the procedures in this chapter to identify the source of problems.

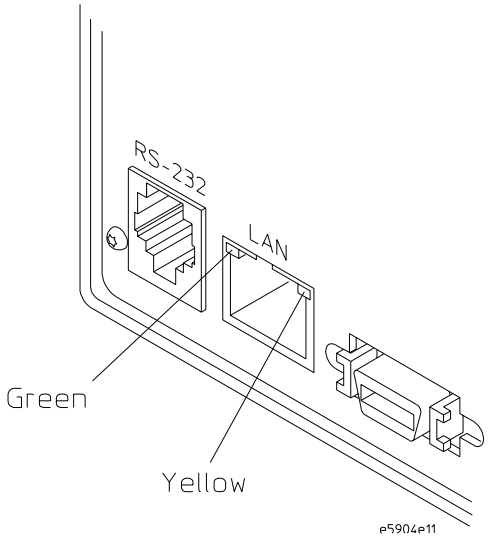
Interpreting the Trace Port Analyzer Status Lights

Power ON Light



The green LED, to the left of the power switch, is lit when the trace port analyzer is connected to a power source and the power switch is on.

LAN Status Lights

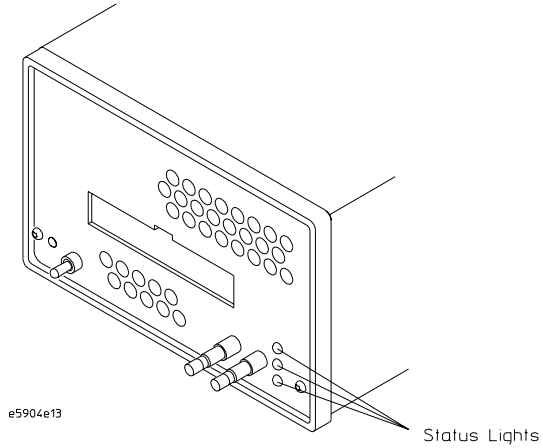


The yellow LED, on the right side of the connector, indicates LAN activity (receive or transmit).

The green LED, on the left side of the connector, is lit when the LAN interface is operating in 100BASE-TX mode.

Target System Status Lights

The trace port analyzer uses status lights to communicate various modes and error conditions. The following table gives more information about the meaning of the power and target system status lights.



❍ = LED is off ● = LED is on

Power/Target System Status Lights

❍ RST ❍ DBG ❍ RUN	No power to the target system, or trace port analyzer is not connected to the target system
● RST ❍ DBG ❍ RUN	Target system is in a reset state
❍ RST ● DBG ❍ RUN	The target system processor is in Debug Mode
❍ RST ❍ DBG ● RUN	The target system processor is executing user code
❍ RST ● DBG ● RUN	Only boot firmware is good (other firmware has been corrupted)
● RST ● DBG ● RUN	The trace port analyzer can no longer control the target system. Reset the target system; then, initialize the trace port analyzer.

Verifying Trace Port Analyzer LAN Communications

Follow these steps if there are problems establishing LAN communications to the trace port analyzer from a debugger or by using telnet on a networked computer.

Step 1. Verify the physical connection

1. Make sure that the proper LAN cable is connected.
   - Use a Category 5 cable if your connection is running at 100 Mbps (100BASE-TX).
   - Use a Category 3 cable if your connection is running at 10 Mbps (10BASE-T).
2. With the trace port analyzer powered on, look at the LAN status lights to verify that the trace port analyzer is seeing LAN activity.

   See “LAN Status Lights” on page 104. No activity indicates a problem with the LAN port or cable. Contact your network system administrator.

Step 2. Use the “ping” command on a networked computer

These instructions assume you are using a personal computer running Microsoft® Windows®. The procedure for other operating systems is slightly different.

1. Open an MS-DOS Command Prompt window, or choose Start->Run....
2. Enter the “ping” command followed by the IP address of the trace port analyzer.

Example

```
C:\WINDOWS>ping 192.35.12.6
```

```
Pinging 192.35.12.6 with 32 bytes of data:

Reply from 15.6.253.138: bytes=32 time=1ms TTL=254
Reply from 15.6.253.138: bytes=32 time=1ms TTL=254
Reply from 15.6.253.138: bytes=32 time=1ms TTL=254
Reply from 15.6.253.138: bytes=32 time<10ms TTL=254
```

3 If ping gets replies from the trace port analyzer (but you are unable to telnet to it), try rebooting the trace port analyzer by turning its power switch off then on again.

Problems with trace port analyzer firmware could lead to situations where the LAN interface is up and running but you are not able to telnet to the trace port analyzer or, if you are able to telnet to the trace port analyzer, you are not able to enter commands.

If there are LAN connection problems

If the results of the "ping" command shows something like "100% packet loss" or "Destination host unreachable":

- ❏ Make sure that you have connected the trace port analyzer to the proper power source and that the power light is lit.
- ❏ Make sure that you wait for the power-on self test to complete before connecting.
- ❏ If you have just changed the IP address of the trace port analyzer, leave the trace port analyzer powered on and connected to the LAN for a few minutes, then try again.

  Some hubs, routers, and hosts maintain tables of IP addresses and link-level addresses. It may take a while for these tables to be updated.

❏ Make sure that the trace port analyzer's IP address is set up correctly.

To do this, repeat the steps shown in "To set LAN parameters using a serial port connection" on page 45.

❏ If the trace port analyzer is on a different subnet than the host computer, make sure that the gateway address is set up correctly.

The default gateway address of 0.0.0.0 does not allow the trace port analyzer to communicate with computers on other subnets.

If it takes a long time to connect to the network

❏ Check the subnet masks on the other LAN devices connected to your network. All of the devices should be configured to use the same subnet mask.

Subnet mask error messages do not indicate a major problem. You can continue using the trace port analyzer.

If there are many subnet masks in use on the local subnet, the trace port analyzer may take a very long time to connect to the network after it is turned on.

Checking the Initial Trace Port Analyzer Status

After establishing a telnet connection to the trace port analyzer, an initial status prompt of “->” or “?>” indicates a problem.

If the prompt is “->”

The "->" prompt indicates that the trace port analyzer is not connected to a target probe (which is the 60-pin cable and a buffer board) or that the firmware loaded into the trace port analyzer is not compatible with its hardware.

Try one of the following until you get a different prompt:

- ❏ If the trace port analyzer is not connected to the target probe, connect the target probe and enter the “init -c” command to re-initialize.
- ❏ Cycle power on the trace port analyzer. (Turn off target system power first.)
- ❏ Check that the proper firmware is installed by entering the “ver” command.

  The proper firmware is installed at the factory but it could accidentally be changed. If the firmware is incorrect, refer to Chapter 8, “Updating Firmware,” on page 97.

If the prompt is “?>”

The "?>" prompt indicates that the trace port analyzer is having trouble communicating with the target system. The trace port analyzer doesn’t know what state the target system is in.

❑ Follow the procedure in the “Verifying Run Control Interaction with the Target System” on page 111.

Verifying Run Control Interaction with the Target System

Use the following procedure to verify that the trace port analyzer's run control port is operating properly with the target system.

Connection to the wrong target system or connection to a target system whose pins are connected backward could potentially damage the trace port analyzer.

Step 1. Initialize the trace port analyzer

1. Follow the procedure in Chapter 6, "Connecting to a Target System," on page 85.
2. Telnet to the trace port analyzer.
3. Initialize the trace port analyzer by entering the "init -c" command.

   ```
   ?>init -c
   ```

   You can enter this command at any prompt. This command will set the default configuration settings and will display the same information as the "ver" command.

   The initial prompt can be used to diagnose several common problems.

   If the initial prompt is "R>", the trace port analyzer is scanning the JTAG interface correctly. Go to "Step 2. Configure the trace port analyzer" on page 113.

If the response is "!ERROR 905!"

If the response is "!ERROR 905! Driver firmware is incompatible with ID of attached device":

❏ Make sure the correct firmware is loaded into the trace port analyzer.

See "To display current firmware version information" on page 98.

If the initial prompt is "p>"

❏ Make sure that the target system is powered on and that the VTRef pin on the target system header connector has the proper reference voltage.

If the initial prompt is "M>"

❏ The processor entered debug mode without the help of the trace port analyzer. Is another debugger connected?

If the initial prompt is "?>"

❑ Check TCK, TDO, TDI, TMS, and nTRST signals. Check the firmware revision.

Check the logic levels on the target system's debug port. See also "Required Voltage Levels: 3.3 V - 5.5 V Buffer Board" on page 32 or "Required Voltage Levels: 3.3 V - 5.5 V Buffer Board" on page 32.

Signal Levels with the trace port analyzer in default[1] reset state

Signal Name	Level
VTref	See page 31 or 32.
TDI	Toggling
TDO	Toggling
TCK	~32 MHz signal[2]
TMS	Toggling
SRESET	Low
HALT	High
nTRST	High

All other pins should be low.

[1]Default cf settings

[2] Default is 32 MHz. Actual value depends on JTAG speed setting (see page 67).

If the run control port signals are okay and the prompt is still "?>", refer to "If the trace port analyzer has problems controlling the target system" on page 118.

Step 2. Configure the trace port analyzer

- Configure the trace port analyzer appropriately for the target system.

See Chapter 5, "Configuring the Trace Port Analyzer," on page 61.

If the appropriate configuration options were previously saved with the "cfsave -s" command, you can restore them with the "cfsave -r" command.

Step 3. Enter the reset command

- Enter the "rst" command:

```
R>rst
R>
```

The "R>" prompt is a good response that indicates that nRESET is working. Go to "Step 4. Enter the run command" on page 114.

Step 4. Enter the run command

- Enter the "r" command:

```
R>r
U>
```

If the prompt after the run command is "U>" with no error messages, everything is still working correctly. Go to "Step 5. Enter the break command" on page 114.

Step 5. Enter the break command

- Enter the "b" command:

```
U>b
M>
```

If the prompt after the break command is "M>" with no error messages, everything is still working correctly. Go to "Step 6. Check register and memory access" on page 115.

If the prompt is "U>" with error messages

- ❏ If you see "!ERROR 608! Unable to break", make sure the processor type configuration option is set correctly.
- ❏ If "!ERROR 608! Unable to break" still occurs, reduce JTAG communication speed (see page 67).
- ❏ Reset (or cycle power on) the target system.
- ❏ Make sure you are using the command sequence:

```
U>rst
R>r
U>b
M>
```

  Some PowerPC chips have problems if JTAG commands are issued while the chip is reset. Using the "rst", "r", "b" sequence avoids this problem.

- ❏ If the problem persists, see "If the trace port analyzer has problems controlling the target system" on page 118.

Step 6. Check register and memory access

1 At the "M>" prompt, check register accesses:

```
M>reg r0
  reg r0=xxxxxxxx
M>reg r0=12345678
M>reg r0
  reg r0=12345678
M>
```

If the value read is equal to the value written, the voltage level of the chip is probably correct.

2 Before checking memory accesses, set caches and translation off.

For information on doing this, refer to the documentation for the target system.

3 Check memory accesses:

```
M>m -d4 -a4 0=11111111,22222222,33333333,44444444
M>m -d4 -a4 0..
  00000000   11111111 22222222 33333333 44444444
  00000010   00000000 00000000 00000000 00000000
  00000020   00000000 00000000 00000000 00000000
  00000030   00000000 00000000 00000000 00000000
  00000040   00000000 00000000 00000000 00000000
  00000050   00000000 00000000 00000000 00000000
  00000060   00000000 00000000 00000000 00000000
  00000070   00000000 00000000 00000000 00000000
M>
```

If the values read are equal to the values written, memory is working. Go to "Step 7. Run a short program" on page 116.

If you see memory-related problems

❑ If the value read is not equal to the value written, it implies that the memory controller may not be initialized.

Be sure the memory controller for your target system is setup correctly.

Step 7. Run a short program

To more fully test your target, you can load simple programs into memory and execute them.

1 Modify memory locations to load a short program:

```
M>m -d4 -a4 100=38210001,60000000,48000102
M>reg r1=0
M>
```

In assembly language this is:

```
addi r1, r1, 1
ori  0, 0, 0
ba   100
```

2 Set the program counter register to the address of the short program:

```
M>reg pc=100
M>
```

3 Step the program; then, check the register contents:

```
M>s
  PC = 00000104
M>reg r1
  reg R1=00000001
M>
```

This should return "reg R1=00000001"

NOTE: Stepping can fail if memory at the current program counter does not contain a valid instruction.

4 Verify the register increments after every three steps:

```
M>s 3
  PC = 00000100
M>reg r1
  reg R1=00000002
M>
```

If the program does not execute correctly

If this does not work as described, make sure the memory at 100 is read/write memory, and that the memory controller is programmed correctly.

If the trace port analyzer has problems controlling the target system

The trace port analyzer might be having problems controlling the target if you see messages such as:

"!ERROR 608! Unable to break"

Or the prompt changes to "?>"

Problems controlling the target can be caused by a variety of conditions. Typically the problem is in the configuration of the trace port analyzer or the configuration of the target system.

Try the following to better control your target system:

- ❏ Decrease the JTAG communication speed. Some target systems need slower speeds to properly communicate.

  Use the **`cf speed`** command (see "To specify the JTAG clock speed" on page 67).

- ❏ Check the trace port analyzer configuration settings.

  Enter the **`cf`** command to display the configuration settings (see "Using the Built-In "cf" Command" on page 63).

- ❏ Check that the trace port analyzer is not restricted to real-time runs.

  If you are using a telnet connection or a debugger command file, use the **`cf rrt=no`** command.

  Restricting to real-time runs will not allow you to access memory or registers while the target system program is running. By setting this option to "no", you will be able to access the memory and registers while the target system program is running.

- ❏ Check that the target system processor is configured.

  Some devices under test require configuration registers on the processor to be initialized before the trace port analyzer can properly communicate with the target system.

  For example, some processors need their memory controllers initialized.

  To initialize the target processor, either run the target system from reset (if you have a BOOT ROM) or define a series of trace port analyzer commands to initialize the target system.

- ❏ Check that the proper firmware is installed by entering the "ver" command (see "To display current firmware version information" on page 98).

  The proper firmware is installed at the factory but it could accidentally be changed. If the firmware is incorrect, refer to Chapter 8, "Updating Firmware," on page 97.

Contacting Agilent Technologies

If the trace port analyzer still does not work after following the troubleshooting steps in this chapter:

1. Write down the target processor version, the trace port analyzer firmware version, and the trace port analyzer model number (Agilent Technologies E5904B Option 060).
2. Call your nearest Agilent Technologies sales or service office.

   To locate a sales or service office near you, go to the world-wide web site:

   http://www.tm.agilent.com

   and select Contact Us.

10

Characteristics

This chapter describes the following characteristics of the Agilent Technologies E5905B Option 060 trace port analyzer:

- Input/output electrical characteristics.
- Run control unit characteristics.
- Trace port analysis characteristics.
- Environmental characteristics.

Input/Output Electrical Characteristics

Trigger Out SMB Port

With a 50 Ω load, a logic high is ≥ 2.0 V, and a low is ≤ 0.4 V. The output function is selectable (see "To configure the Trigger Out SMB port" on page 78).

Break In SMB Port

Edge-triggered TTL level input, 20 pF, with 4.6 kΩ to ground in parallel. Maximum input: +5 V to -5 V when the trace port analyzer is powered OFF; +10 V to -5 V when the trace port analyzer is powered ON. Input function is selectable (see "To configure the Break In SMB port" on page 77).

Communication Ports

Serial Port

RJ12 connector (DB9-to-RJ12 adapter and serial cable included). RS-232 DCE to 115.2 kbaud.

IEEE 802.3 Type 10/100Base-TX LAN Port

RJ-45 connector, is compatible with both 10 Mbps (10Base-T) and 100 Mbps (100Base-TX) twisted-pair ethernet LANs.

Power Supply

Input. 100-240 V, 1.0 A, 50/60 Hz, IEC 320 connector.

Output. 12 V, 3.3 A

CAT I (Mains isolated).

Run Control Unit Characteristics

Processor Compatibility

The Agilent Technologies E5904B Option 060 trace port analyzer supports the processors and ASIC cores listed in "Processors and ASIC Cores Supported" on page 4.

Electrical Characteristics

Input Characteristics							
Signal	**Symbol**	**1/3 VTref**		**1/2 VTref**		**2/3 VTref**	
		Min	**Max**	**Min**	**Max**	**Min**	**Max**
TDO	Vih	0.5 VTref	5.1 V	0.65 VTref	5.1 V	0.8 VTref	5.1 V
	Vil	-0.1V	0.2 VTref	-0.1 V	0.35 V	-0.1 V	0.5 VTref
	Ib (Bias)	± 15 uA					
	Rin	4.7 kΩ pullup to VTref					
	Cin	TDO = 75 pF, RTCK = 80 pF					

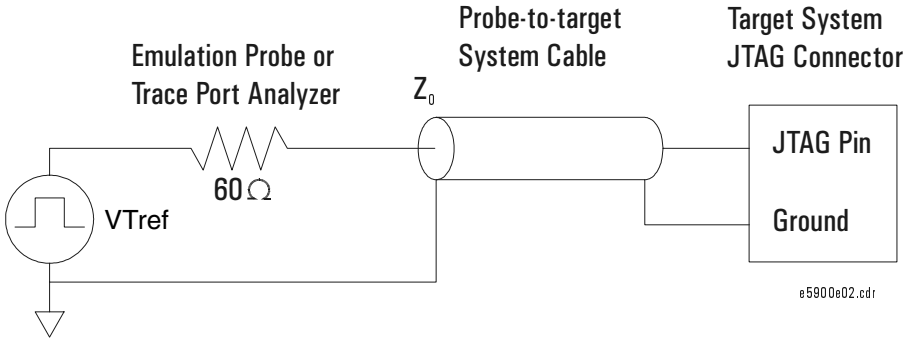
Input Characteristics			
Signal	**Symbol**	**Min**	**Max**
VTref[1]	Vin	1.65 V	3.6 V
	Rin	25 kΩ pulldown to ground	
$\overline{\text{SRESET}}$	Rin (inactive)	4.7 kΩ pullup to VTref	
	Rin (active)	12 Ω pulldown to ground	
	Cout		200 pF
	Vin		5.5 V

[1] VTref is used to determine the target power status and the reference for input threshold and output voltage swings. The trace port analyzer does not draw power from this source.

Output Signal Characteristics		
Signal	**Symbol**	**Condition**
TDI,TCK,TMS,$\overline{\text{TRST}}$	Voh/Ioh	66 Ω ± 15 Ω to VTref
	Vol/Iol	66 Ω ± 15 Ω to 0.2 V

Output Model

Model of output drive to TDI, TCK, TMS, TRST and HALT.



Note: Z_o = 66 Ω in the diagram above.

Trace Port Analysis Unit Characteristics

For the characteristics of the trace port analysis unit, see:

- "Signal Requirements" on page 30.
- "Required Voltage Levels: 1.8 V - 3.3 V Buffer Board" on page 31.
- "Required Voltage Levels: 3.3 V - 5.5 V Buffer Board" on page 32.
- "Loading Effects" on page 33.

Environmental Characteristics

Temperature	Operating: +5 degrees to +40 degrees C (+41 to +104 degrees F) Non-operating: -40 degrees to +70 degrees C (-40 to +158 degrees F).
Relative Humidity	15% to 95%
Pollution Degree	Pollution degree 2: Normally only dry non-conductive pollution occurs. Occasionally a temporary conductivity caused by condensation may occur.
Altitude	Operating or non-operating: 4600 m (15 000 ft.).
For indoor use only.	

EMC

	Performance Criteria
IEC 61326-1:1997+A1:1998 / EN 61326-1:1997+A1:1998	
CISPR 11:1990 / EN 55011:1991– Group 1 Class A	A [See Note]
IEC 61000-4-2:1995+A1:1998 / EN 61000-4-2:1995 (ESD 4kV CD, 8kV AD)	A
IEC 61000-4-3:1995 / EN 61000-4-3:1995 (3V/m 80% AM)	A
IEC 61000-4-4:1995 / EN 61000-4-4:1995 (EFT 0.5kV line-line, 1kV line-earth)	A
IEC 61000-4-6:1996 / EN 61000-4-6:1996 (3V 80% AM, power line)	A
Australia/New Zealand: AS/NZS 2064.1	
Canada: ICES-001:1998	

Safety

IEC 61010-1:1990+A1:1992+A2:1995 / EN 61010-1:1994+A2:1995
Canada: CSA C22.2 No. 1010.1:1992
USA: UL 3111-1:1994 {optional}

Additional Information:

The product herewith complies with the requirements of the Low Voltage Directive 73/23/EEC and the EMC Directive 89/336/EEC (including 93/68/EEC) and carries the CE Marking accordingly (European Union).

Performance Criteria:
A Pass - Normal operation, no effect.
B Pass - Temporary degradation, self recoverable.
C Pass - Temporary degradation, operator intervention required.
D Fail - Not recoverable, component damage.

Note:
The target probes (cable plus buffer board) are ESD sensitive. Use standard ESD preventive practices to avoid component damage.

11

Service Guide

To get replacement parts

The following table lists some parts that may be replaced if they are damaged or lost. The part numbers are subject to change. Contact your nearest Agilent Technologies sales office for further information (see "Contacting Agilent Technologies" on page 160).

Replacement assemblies

Part number	Description
0950-3043	Power supply for trace port analyzer (marked F1044B)
E3483-68700	Ferrite kit for power supply
E5903-61601	60-pin cable
E3483-68700	Ferrite kit for 60-pin cable
E5903-66503	1.8 V - 3.3 V buffer board
E5903-66502	3.3 V - 5.0 V buffer board
E8130-68702	Serial cable and adapter

NOTE: See the figure on page 5 for an illustration of most of these replacement parts.

To exchange a faulty assembly for a repaired and tested assembly

The following item has been set up on the Agilent Technologies exchange assembly program. You can exchange a faulty assembly with one that has been repaired, calibrated, and performance verified by the factory. The cost is significantly less than that of a new assembly.

Exchange assemblies

Part number	Description
E5840-69501	Rebuilt trace port analyzer for ARM (accessories not included)

To return a part to Agilent Technologies for service

1. Follow the procedures in the "Solving Problems" chapter to make sure that the problem is caused by a hardware failure and not by configuration or cabling problems.
2. Get the address of the nearest Agilent Technologies service center.

   See "Contacting Agilent Technologies" on page 120.
3. Package the part and send it to the Agilent Technologies service center.

   Keep any parts which you know are working. For example, if only a cable is broken, keep the trace port analyzer.
4. When the part has been replaced, it will be sent back to you.

   The unit returned to you will have the same serial number as the unit you sent to Agilent Technologies.

   In some parts of the world, on-site repair service is available. Ask an Agilent Technologies sales or service representative for details.

To clean the instrument

If the instrument requires cleaning:

1. Remove power from the instrument.
2. Clean the instrument using a soft cloth that has been moistened in a mixture of mild detergent and water.
3. Make sure that the instrument is completely dry before reconnecting it to a power source.

D

debug port A hardware interface designed into a microprocessor that allows developers to control microprocessor execution, set breakpoints, and access microprocessor registers or target system memory using a tool like the emulation probe.

device under test Another name for a target system under development.

H

hostname A name that is associated with the IP address of a device on the network.

I

IP address An address, in integer dot notation (for example, 15.6.240.253), that is given to a device on the network.

L

LAN name See *hostname*.

R

run control unit A device that connects to a microprocessor's debug port to provide run control features like: starting/stopping program execution, single-stepping through programs, and modifying registers and memory contents.

T

target system The device under test that is being developed and debugged.

threshold voltage The level at which voltages above are logic "highs" (1) and voltages below are logic "lows" (0).

trace port analyzer A tool that collects processor execution information and presents it to a software debugger.

trigger specification A set of conditions that must be true before the instrument triggers.

Index

Agilent

DECLARATION OF CONFORMITY

According to ISO/IEC Guide 22 and CEN/CENELEC EN 45014

Manufacturer's Name: Agilent Technologies, Inc.
Manufacturer's Address: 1900 Garden of the Gods Road
Colorado Springs, Colorado
80907 U.S.A.

Declares, that the product

Product Name: Trace Port Analyzer

Model Number: E5904B (E3483B)

Product Options: This declaration covers all options of the above product(s).

Conforms with the following product standards:

EMC	Standard	Limit
	IEC 61326-1:1997+A1:1998 / EN 61326-1:1997+A1:1998	
	CISPR 11:1990 / EN 55011:1991	Group 1 Class A [1]
	IEC 61000-4-2:1995+A1:1998 / EN 61000-4-2:1995	4kV CD, 8kV AD
	IEC 61000-4-3:1995 / EN 61000-4-3:1995	3V/m, 80-1000 MHz
	IEC 61000-4-4:1995 / EN 61000-4-4:1995	0.5kV signal lines, 1kV power lines
	IEC 61000-4-6:1996 / EN 61000-4-6:1996	3V, 0.15-80 MHz
	Canada: ICES-001:1998	
	Australia/New Zealand: AS/NZS 2064.1	
Safety	IEC 61010-1:1990+A1:1992+A2:1995 / EN 61010-1:1993+A2:1995	
	Canada: CSA C22.2 No. 1010.1:1992	

Conformity / Supplemental Information:

The product herewith complies with the requirements of the Low Voltage Directive 73/23/EEC and the EMC Directive 89/336/EEC (including 93/68/EEC) and carries the CE Marking accordingly (European Union).

[1] The product was tested in a typical configuration with Agilent Technologies test systems.

Date: 8/24/2000

Ken Wyatt
Name

Ken Wyatt / Product Regulations Manager

For further information, please contact your local Agilent Technologies sales office, agent or distributor.

Product Regulations

EMC	IEC 61326-1:1997+A1:1998 / EN 61326-1:1997+A1:1998	Performance Criteria
	CISPR 11:1990 / EN 55011:1991– Group 1 Class A	
CE	IEC 61000-4-2:1995+A1:1998 / EN 61000-4-2:1995 (ESD 4kV CD, 8kV AD)	A (See Note)
	IEC 61000-4-3:1995 / EN 61000-4-3:1995 (3V/m 80% AM)	A
ISM 1-A	IEC 61000-4-4:1995 / EN 61000-4-4:1995 (EFT 0.5kV line-line, 1kV line-earth)	A
	IEC 61000-4-6:1996 / EN 61000-4-6:1996 (3V 80% AM, power line)	A
N10149	Australia/New Zealand: AS/NZS 2064.1	
	Canada: ICES-001:1998	

Safety	IEC 61010-1:1990+A1:1992+A2:1995 / EN 61010-1:1994+A2:1995
	Canada: CSA C22.2 No. 1010.1:1992
	USA: UL 3111-1:1994 {optional}

Additional Information:

The product herewith complies with the requirements of the Low Voltage Directive 73/23/EEC and the EMC Directive 89/336/EEC (including 93/68/EEC) and carries the CE Marking accordingly (European Union).

Performance Criteria:

A Pass - Normal operation, no effect.
B Pass - Temporary degradation, self- recoverable.
C Pass - Temporary degradation, operator intervention required.
D Fail - Not recoverable, component damage.

Note:

The target probes (cable plus buffer board) are ESD sensitive. Use standard ESD preventive practices to avoid component damage.

Sound Pressure Level N/A

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Warning

- Before turning on the instrument, you must connect the protective earth terminal of the instrument to the protective conductor of the (mains) power cord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. You must not negate the protective action by using an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two-conductor outlet is not sufficient protection.
- Only fuses with the required rated current, voltage, and specified type (normal blow, time delay, etc.) should be used. Do not use repaired fuses or short-circuited fuseholders. To do so could cause a shock of fire hazard.
- Service instructions are for trained service personnel. To avoid dangerous electric shock, do not perform any service unless qualified to do so. Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.
- If you energize this instrument by an auto transformer (for voltage reduction), make sure the common terminal is connected to the earth terminal of the power source.
- Whenever it is likely that the ground protection is impaired, you must make the instrument inoperative and secure it against any unintended operation.
- Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.
- Do not install substitute parts or perform any unauthorized modification to the instrument.
- Capacitors inside the instrument may retain a charge even if the instrument is disconnected from its source of supply.

Safety Symbols

Instruction manual symbol: the product is marked with this symbol when it is necessary for you to refer to the instruction manual in order to protect against damage to the product.

Hazardous voltage symbol.

Earth terminal symbol: Used to indicate a circuit common connected to grounded chassis.

WARNING

The Warning sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a Warning sign until the indicated conditions are fully understood and met.

CAUTION

The Caution sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a Caution symbol until the indicated conditions are fully understood or met.

Agilent Technologies
P.O. Box 2197
1900 Garden of the Gods Road
Colorado Springs, CO 80901-2197, U.S.A.

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About this edition

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